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Thermal Resistance of Low Power Semiconductor Devices under Pulse Conditions

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To protect the junction of a semiconductor device, manufacturers usually stipulate a maximum junction temperature for that device. Under pulsed-current conditions the thermal capacitances of the whole semiconductor device tend to limit the temperature changes at the junction. Thus the relevant data for calculating steady state junction temperatures introduces unnecessarily large safety factors if used for pulses. The present article describes a method of measuring junction temperature, and uses the concept of transient thermal resistance in such a way that the junction temperature under pulse conditions can be calculated. A practical example is given to show how the junction temperature of a pulsed transistor can be calculated by the method described.

INTRODUCTION

When the power handling capacity of a semiconductor device is estimated by the manufacturer before the relevant data is published, the fundamental restriction which is observed is that of the temperature of the semiconductor junction. Exceeding this maximum temperature rating could lead to damage within the device, and sometimes even to immediate catastrophic failure. To help circuit designers observe this absolute maximum rating, without having to measure the junction temperature itself, the published data has provided information which can be used to calculate conditions under which no damage will occur. The relevant information given includes an absolute maximum power and junction temperature, a value of the steady state thermal resistance, and an equation relating total power to the maximum junction temperature, and to either the case temperature or the ambient temperature. Under pulsed conditions, however, it is possible for the peak power to exceed the steady state maximum, provided that the peak does not last long enough to cause the junction temperature to exceed its rating. Therefore, the information given to safeguard the device under pulsed conditions includes a maximum averaging time for the current rating, or pulse rating charts. These charts are for establishing suitably modified values of thermal resistance for calculations based on various pulse conditions. The derivation of these modified values of thermal resistance is the topic of this present article. The article is complementary to a previous article on steady state thermal resistance (Ref. 4), and the procedures for examining junction temperature are similar in both.

Steady-state Thermal Resistance

When there is steady dissipation, in which dynamic equilibrium of heat flow from the junction to the ambient is reached, the thermal path may be considered to be a simple network of thermal resistances. In these circumstances the junction temperature is given by the simple expression:

$$T_j = T_{amb} + P.\theta \qquad \ldots(1)$$

where

T_j = junction temperature,
T_{amb} = ambient temperature,
P = steady state dissipation,
θ = steady state thermal resistance between junction and ambient.

However, thermal capacitance is associated with the several regions of the device. Thus the junction temperature response following a power step is a function of time. In particular, the maximum temperature reached under pulsed load conditions is lower than for the same power level operating continuously, if the pulse-duration is less

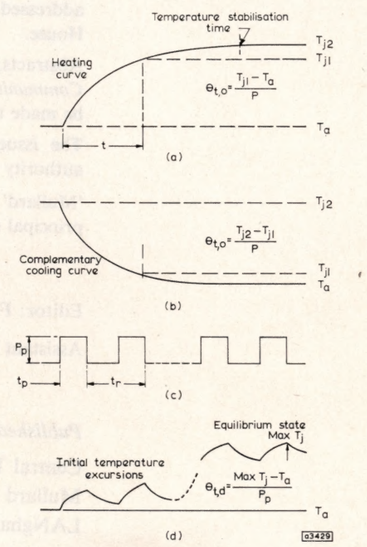


Fig. 1—Junction temperature response

than 'the stabilisation time'. Hence, to produce an expression comparable to Eq.(1) above, and applicable to these conditions, the concept of transient thermal resistance, which is also a function of time, is used.

CONCEPT OF 'TRANSIENT' THERMAL RESISTANCE

When a step function of power is applied to a device, the response of its junction temperature is of the general form shown in Fig. 1. For this single step function the concept of 'transient' thermal resistance (designated $\theta_{t,0}$) may be used to correlate the junction temperature at any instant and the magnitude of the power step. The value of $\theta_{t,0}$ at this instant is defined as the ratio of the change of temperature at the time 't' after the power step to the change in power. Thus, $\theta_{t,0}$ is a monotonic parameter, increasing with time in exactly the same manner as the heating curve. The single power step is rarely encountered in practice, but the response to this step will be shown later to be of considerable importance.

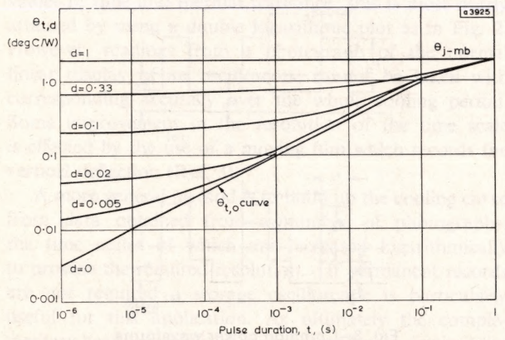


Fig. 2—Typical curves of transient θ against pulse duration

The concept of transient thermal resistance can be extended to embrace the more usual case of a train of rectangular power pulses, and the symbol $\theta_{t,d}$ is used. This is defined as the ratio of the maximum temperature rise encountered to the magnitude of the power steps producing the rise. The maximum temperature rise, and hence $\theta_{t,d}$, depend on both the pulse duration, t_p, and the duty cycle, d. The value of d is given by the equation $d = t_p/t_r$, where t_r is the periodic time. The value of $\theta_{t,d}$ lies between the limits $\theta_{t,0}$ and θ. If the cooling period $(t_r - t_p)$ is greater than the temperature stabilisation time, t_s, the junction always cools to its initial value between each pulse, and the temperature response is the same as that for a single step; that is, $\theta_{t,d} = \theta_{t,0}$. If the heating time t_p is greater than the temperature stabilisation time, the steady state junction temperature is reached; that is, $\theta_{t,d} = \theta$. For cooling periods shorter than t_s the junction will not cool to its initial value and so the temperature excursions are superimposed on progressively higher values; this will continue until the temperature rise during the dissipating period is equal to the fall in temperature during the off period. The temperature at the end of any pulse after this quasi-equilibrium state has been reached is the maximum for this operation.

DERIVATION OF INFORMATION

Three methods of examining the transient thermal resistance are now described. The third method combines the two other procedures.

Theoretical Approach

If the heating curve of a semiconductor junction following a step function of power (Fig. 1) could be regarded as a single exponential function, and if the initial and final temperatures were known, the specification of the thermal time constant would define the curve uniquely. With such a simple approximation the thermal response to power pulse trains could easily be calculated.

However, theoretical calculations considering one-dimensional heat flow indicate a more complex function (Ref. 1), in which the rate of increase in temperature is initially larger, such that the curve lies above that expected for exponential behaviour. This leads to a new definition of the time constant to be used in conjunction with this function: the time constant is that period required for the junction temperature to rise to 70% of its overall change as contrasted with approximately 63% for the true exponential.

Extension of the theoretical formula to include the temperature variation under pulsed excitation results in a family of loci relating the pulse duration, duty cycle and transient thermal resistance, as in Fig. 2. However, many simplifying assumptions are made in the theoretical transistor model, and in general theoretical curves tend to give an unduly large safety factor.

Practical Approach

The direct practical method of determining the transient thermal resistance is to measure the actual junction temperature rise for specified values of pulse duration, duty cycle and pulse power. By making a large number of individual measurements the pulse rating chart for a single transistor may be built up. Such a chart, being based on one sample, cannot be used as a general rating for any particular type of device as the spread for many devices must be taken into account. In addition, life tests based on the pulse power calculated from the chart should indicate satisfactory serviceability of the device.

This method has been used to check the curves obtained otherwise, but it is a tedious method of producing a full chart. It may be used to advantage, however, when an indication for a specific application is required.

Combined Approach

The basis of this approach is that the transient thermal resistance can be calculated from a knowledge of that for a single step in power, that is the curve corresponding to $d = 0$. From the principle of the superposition of positive and negative power steps (Ref. 2), the following relation has been derived (see Appendix 2).

$$\theta_{t_p,d} = d.\theta + (1-d)\theta_{(t_r+t_p),0} + \theta_{t_p,0} - \theta_{t_r,0} \qquad \ldots(2)$$

where $\theta_{t_i,0}$ is the transient thermal resistance at the instant t_i. In this case, only the single step response curve need be measured.

USE OF INFORMATION

The information derived from the above calculations may be used in several ways. These are discussed below.

Calculation of Junction Temperature

Let us consider the three common repetitive power waveforms shown in Fig. 3.

Case 1

A power pulse train of magnitude P_p (Fig. 3a) is dissipated in a device mounted on an infinite heatsink. The maximum junction temperature is then given by the equation

$$T_j = T_{amb} + P_p\theta_{t,d} \quad \ldots(3)$$

Under practical conditions, when the device is mounted on a heatsink of thermal resistance θ_h with an interface thermal resistance of θ_i, the term $d(\theta_h+\theta_i)P_p$ must be added. This is the rise in temperature of the mounting base due to the transmission of the average power to the ambient. Equation (3) then becomes

$$T_j = T_{amb} + P_p[\theta_{t,d} + d(\theta_h+\theta_i)] \quad \ldots(4)$$

Case 2

The above power train is superposed on a steady dissipation level P (Fig. 3b). The maximum junction temperature is then given by

$$T_j = T_{amb} + P_p\theta_{t,d} + d.(\theta_h+\theta_i) + P.\theta_{j\text{-}amb} \quad \ldots(5)$$

Case 3

The waveform in case 1 is superposed on a second repetitive rectangular waveform (see Fig. 3c) having the same repetition time but different pulse duration. It is important that individual pulses of each train finish simultaneously. Using the principle of superposition, the maximum junction temperature of a device mounted on an infinite heatsink is given by

$$T_j = T_{amb} + P_{p1}\theta_{t1,d1} + P_{p2}\theta_{t2,d2} \quad \ldots(6)$$

Where P_p, t_1, d_1 are the magnitude, pulse duration and duty cycle respectively of the first pulse train, and P_{p2}, t_2, d_2 the corresponding values of the superposed pulse train.

On a practical heatsink as in case (1) we have

$$T_j = T_{amb} + P_{p1}\theta_{t1,d1} + P_{p2}\theta_{t2,d2} + (d_1P_{p1} + d_2P_{p2})(\theta_h+\theta_i) \quad \ldots(7)$$

If further, these trains are also superposed on a steady power P, the term $P.\theta_{j\text{-}amb}$ is simply added.

All the terms in the above expressions except $\theta_{t,d}$ are defined uniquely. $\theta_{t,d}$ may be found from the published data in two ways: if the relevant value of d is not one of the curves plotted, a rough interpolation may be made, or alternatively the following equation is provided which may be used to calculate $\theta_{t,d}$ from the corresponding value of $\theta_{t,0}$:

$$\theta_{t,d} = d(\theta_{j\text{-}mb} - \theta_{t,0}) + \theta_{t,0} \quad \ldots(8)$$

(this is compared with Eq.17 in Appendix 2).

This equation can be used to advantage as follows.

In case 2 above, Eq.(5) can be rewritten by substitution of $\theta_{t,d}$

$$\begin{aligned} T_j &= T_{amb} + P_p[d(\theta_{j\text{-}mb} - \theta_{t,0}) + \theta_{t,0}] + d(\theta_h+\theta_i) + P\theta_{j\text{-}amb} \\ &= T_{amb} + P_p(1-d)\theta_{t,0} + (P+dP_p)\theta_{j\text{-}amb} \\ &= T_{amb} + P_p(1-d)\theta_{t,0} + P_{av}\theta_{j\text{-}amb} \end{aligned} \quad \ldots(9)$$

Similarly, equation (7) can be simplified to

$$T_j = T_{amb} + P_{p1}(1-d_1)\theta_{t1,0} + P_{p2}(1-d_2)\theta_{t2,0} + P_{av}\theta_{j\text{-}amb} \quad \ldots(10)$$

In these two equations the pulse components are separated entirely from the steady state thermal resistance

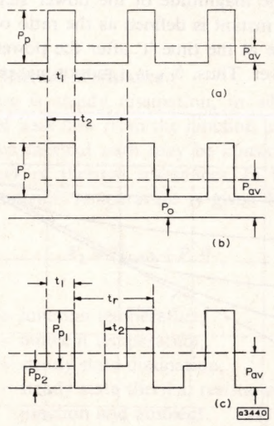


Fig. 3—Common power waveforms

and average power, $\theta_{t,0}$ is the quantity required from the chart, and separation of the components of $\theta_{j\text{-}amb}$ is not required.

In many practical cases the waveform is not a rectangle and the reader is referred to Appendices 3 and 4 for treatment of these conditions.

MEASUREMENT OF TRANSIENT THERMAL RESISTANCE

Throughout the above the quantities required from the chart, either $\theta_{t,d}$ or $\theta_{t,0}$, refer to the internal component of the thermal path. In general the internal heat transfer is predominantly by conduction, and this linear process ensures that the several temperature gradients, consequent on a step of power, follow the same relative changes with time irrespective of the magnitude or sign of the power step. In particular, the heating and cooling responses between two steady temperatures are complementary when the device is mounted on an infinite heatsink.

External quantities, such as the thermal path through heatsinks and mica washers, are assumed invariable in pulsed operation, since by the presence of the relatively large thermal capacitance of the envelope the heat waves are smoothed out to present a steady heat flow. As with normal continuous dissipation conditions, even with a specified mounting, variations in the external thermal resistance do occur at different power levels because of variable convective and radiative effects.

Thus, to produce standard measurements, using either the heating or cooling curve, the test devices are mounted on large heatsinks. Where necessary a temperature correction may be made by monitoring the mounting base, such that the infinite heatsink conditions are simulated.

The Cooling Curve

A known power is dissipated in the device until the equilibrium state is reached; when the load is removed the cooling is observed by monitoring the corresponding response of a temperature sensitive parameter (t.s.p.). By subtracting the cooling curve from its initial maximum value the complementary heating curve, from which $\theta_{t,0}$ is derived, is obtained. (See Fig. 16).

A linear presentation of information is desirable to provide similar percentage reading accuracies for all values of time and thermal resistance; this is most nearly attained by using a double logarithmic plot as in Fig. 2. However, readings from a photograph of the normal linear display of an oscilloscope cannot be taken with corresponding accuracy over the whole cooling period. Some improvement in the resolution of the time scale is effected by the use of a moving film which records the vertical deflection (Ref. 3).

A more general method is to build up the cooling curve from data obtained from a number of photographs, the time scales of which are increased logarithmically to provide the required resolution. If permanent records are not required a storage oscilloscope is particularly useful for this application. As ultimately the complementary heating curve is required, any error in determining the maximum temperature will be common to all points, though particularly significant in the initial cooling period. This value is best derived from the display which covers the shortest period and consequently has the highest resolution. It is assumed that this maximum temperature is common to all displays, since with the longer periods the resolution in this region is inadequate to check any possible deviation. In practice, any variations in ambient conditions will produce corresponding variations in the 'equilibrium' temperature which must be reached before each display.

Corresponding improvement in the resolution of the temperature scale necessary for the double logarithmic presentation is possible in the above method by using higher amplification for the smaller temperature changes recorded in the shorter periods. This, however, places greater reliance on the linearity and the knowledge of the amplification factor of any amplifiers; furthermore practical difficulties are encountered in positioning the trace.

The Heating Curve

Unlike the cooling curve, the heating curve cannot be monitored directly since in practice the t.s.p. (forward voltage at constant current) cannot be accurately observed during dissipation. However, if the t.s.p. is monitored immediately after the load has been removed, the junction temperature relevant to the dissipation period may be determined. Hence any point on the heating curve corresponding to a specified dissipating period may be plotted, and the composite curve can be built up by a number of separate measurements. For the normal presentation the dissipating periods are increased to provide information at equal logarithmic intervals on the time scale.

With the composite cooling curve, a standard temperature excursion, limited by the steady-state thermal resistance, must be used. Hence, one is limited to merely providing a higher amplification of the small changes in the t.s.p. at the shorter periods to obtain the required measuring accuracy. The same will apply to measurements of a heating curve. However, one is not limited to the heating curve associated with a fixed magnitude of power step; since the aim is to plot a curve of $\theta_{t,0}$ which is merely a ratio, individual temperature measurements may be made at any required magnitude of power step. Hence with the pulse method, rather than relying on higher amplification of the t.s.p. for the required measuring accuracy, a higher dissipation level is used to produce a greater change in the t.s.p. itself, thus providing greater sensitivity.

It is for this reason that heating measurements are preferred to the determination from the cooling curve. Further, the measuring procedure is very similar to that used in determining steady-state thermal resistance.

PRINCIPLE OF MEASUREMENT

The method of measuring steady-state thermal resistance (Ref. 4) is the basis from which the more complex techniques used in pulse work have been evolved. A summary of the principles involved in this method will therefore simplify subsequent explanations.

Steady-state Thermal Resistance

The steady-state thermal resistance may be simply expressed as the junction temperature rise per unit dissipation. As the junction is inaccessible the temperature must be determined by the use of an internal temperature sensitive parameter. The t.s.p. used is 'the forward voltage at constant current'. This has the following advantages: it is linear over a wide temperature range provided that the ratio of the constant current to the leakage current exceeds 1000, and for all transistors of a given type the calibration figure (typically −2mV/degC) is substantially the same, provided that the initial forward voltage level is the same (Ref. 5).

The first stage of the measurement is to set up an initial reference voltage by passing a small constant current through the device. If the device under test is a diode, the reference voltage is the normal forward voltage (V_f), or if a transistor, V_{be}. When the load current is superimposed on the reference current the resultant change in dissipation will cause the junction temperature to rise.

However, before the t.s.p. can be monitored the load current must be interrupted. If brief interruptions are made periodically the t.s.p. may be observed as the junction becomes progressively hotter. It must be remembered that cooling takes place during these periods, so that, when the equilibrium is reached, the relevant maximum temperature attained is that corresponding to the origin of the cooling transient. With such a pulse train steady state conditions are realised to within 0·5% by using a duty cycle of 0·995. If the pulse repetition frequency is

greater than one cycle per second the visual display of the cooling transients offers two advantages: the need for storage of information is eliminated, and the incremental rises in junction temperature can be followed visually until the stable state is reached. A typical forward voltage waveform is shown in Fig. 4. As the change in forward voltage ΔV is the change between the initial reference level and the origin of the final cooling transient, a d.c. oscilloscope must be used for the display.

The direct determination of ΔV from the oscilloscope is limited in accuracy by the resolution appertaining to the screen size and the possible need for interpolation between graticule markings (Fig. 5a). If a calibrated 'Y' shift is available, interpolation is unnecessary and greater amplification is permissible (Fig. 5b). However, if the 'Y' shift is limited to one or two diameters the comparatively high reference level nevertheless restricts any such amplification.

These oscilloscope limitations are avoided by the use of external amplifier and shift circuits, such that the scope is used as a visual indicator. The use of a null technique, that is – the 'backing off' of the cooling origin to the initial reference level by means of the 'Y' shift (see Fig. 5) – ensures that the amplifier conditions are the same for the two relevant voltage levels, and hence non-linearity of the amplifier is of no significance. A further advantage of this technique is that a fine 'Y' shift control may be followed with a valve voltmeter to give a direct indication of the value of ΔV.

As the waveform during the dissipating period is of no interest, positive clipping is used to prevent the overload of the oscilloscope within this period.

The overall transistor dissipation is given by the expression

$$P = V_{ec}.I_c + V_{eb}.I_b. \qquad \ldots(11)$$

This would require four separate measurements, hence for simplicity the approximation in Eq.(12) is used.

$$P = V_{ec}.I_c. \qquad \ldots(12)$$

This is valid if $I_c \gg I_b$ and $V_{cb} \gg V_{eb}$. This expression has the advantage that, as with a diode, the dissipation is given by two d.c. meter readings.

Transient Thermal Resistance

The determination of the steady-state thermal resistance given above was in fact that of the transient thermal resistance of the device for a duty cycle approaching unity. Consequently, the same temperature measuring technique may be used in determining the transient thermal resistance $\theta_{t,d}$ for pulse trains having other values of d and t_p.

An external pulse generator is used to provide the triggering for the wide range of values of d and t_p required in these measurements. The values may be set by the generator dials and verified if necessary by examination of the oscilloscope display.

As previously mentioned, this system is more suited to the measurement of $\theta_{t,d}$ for a specific value of d and t_p than for producing a complete derating chart by separate measurements at various power levels.

A simple read-out system is desirable in order to provide a rapid computation of the power level for each measurement. An alternative expression for the dissipation is given by

$$P = V_{ce}.I_e - V_{cb}.I_b. \qquad \ldots(13)$$

If the term $V_{cb}.I_b$ is assumed negligible, and $V_{cb} \gg V_{eb}$, the expression may be further approximated to

$$P = V_{cb}.I_e. \qquad \ldots(14)$$

For a typical gain $\beta = 50$, say, this introduces a 2% error, although at high current levels where $\beta = 10$, say, the error is 10% and a correction is then necessary. Hence, if a defined current is switched into the emitter

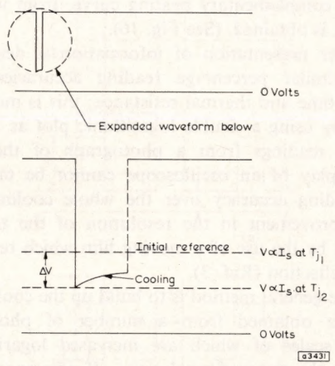


Fig. 4—Typical forward voltage waveform

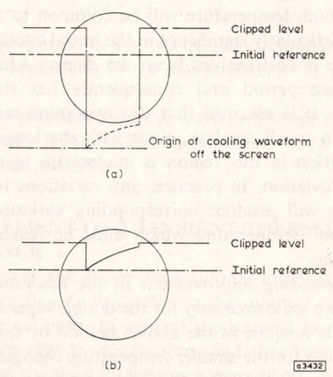


Fig. 5—Oscilloscope display

of the transistor-under-test from an alternative path, the dissipation may be determined from two d.c. meter readings. However, when V_{eb} is significant, a further operation, the reading of V_{eb} from the oscilloscope, is required.

Fast emitter current switching, combined with good amplifier response, ensures that the forward voltage waveform is monitored within a few microseconds of switching. However, it is sometimes impossible to differentiate between a spurious transient and the cooling curve, and, in particular, to determine the origin of cooling. In this case, the junction temperature may not be monitored at the cooling origin but at some time later.

The error introduced by cooling of the junction during this period may be corrected by the following procedure. Using the concept of negative power pulses, we may assume that the original pulse train is composed of two trains (see Fig. 6), one positive with a pulse duration t_1 which includes the original pulse t_p and the extra time required before the measurement, and the other negative with a pulse duration equal to this extra time t_2. We may then write $T_m = P(\theta_{t_1,d_1} - \theta_{t_2,d_2})$, where θ_{t_1,d_1} is the transient thermal resistance of the first component and θ_{t_2,d_2} that of the second.

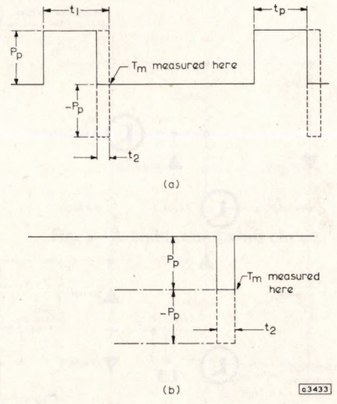


Fig. 6—Delayed temperature measurement

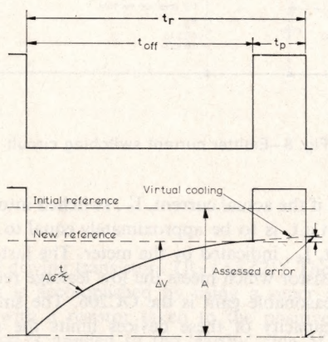


Fig. 7—Assessed error in θ_{t_p} by pulsed method

An approximate value of θ_{t_2,d_2} may be determined by decreasing the pulse duration to t_2, keeping the same pulse repetition frequency. The overall error is then reduced to the error in the correction θ_{t_2,d_2} caused by unobserved cooling. The value of θ_{t_1,d_1} is then determined from the expression given. It must be emphasised that this is not the transient thermal resistance corresponding to the original pulse train but that corresponding to a pulse train having the same pulse repetition frequency and a larger pulse duration ($t_p + t_2$).

This principle may also be applied to the measurement of the steady state thermal resistance θ_{st} (see Fig. 6b). Here a duty cycle close to unity is used, and the cooling or monitoring period is made long enough to ensure that the voltage waveform has become free of spurious transients. If the temperature is measured at the end of this short cooling period we obtain the exact result $T_m = P(\theta_{st} - \theta_{t_2,d_2})$. Again with the knowledge of the value of $\theta_{t_2,0}$ corresponding to the cooling period, we may write

$$\theta_{t_2,d_2} = \bar{d}\theta_{st} + (1-\bar{d})\theta_{t_2,0}$$

where $\bar{d}$ is the complementary duty cycle of the cooling pulses ($\bar{d} = 1-d$).

Thus we have,

$$\frac{T_m}{P} = \theta_{st}(1-\bar{d}) - (1-\bar{d})\theta_{t_2,0}$$
$$= d(\theta_{st} - \theta_{t_2,0}). \qquad \ldots(15)$$

From this equation θ_{st} may be determined.

Single Step Response

It has been mentioned (page 149) that the single step response curve is built up from heating, rather than cooling, measurements. Theoretically a single pulse of power should be used for these measurements, but this entails storage of information and furthermore the null technique may not be used. However, these difficulties may be overcome by modification of the measuring procedure used in the determination of $\theta_{t,d}$ explained above.

A train of power pulses is passed through the device under test: the pulse duration is set to the period required, that is, to t_p for the determination of $\theta_{t_p,0}$; the duty cycle is then adjusted to a value such that, at the end of each cooling period, the junction temperature is near to ambient. When the equilibrium state is reached, that is, when the rise in temperature during a heating pulse is equal to the fall during a cooling period, the level at the end of the cooling periods is taken as the new reference (Fig. 7). If the origin of the cooling waveform is now backed off to this level by the fine 'Y' shift, the voltage change indicated (ΔV) will correspond to the rise in temperature during a single pulse.

The duty cycle setting will determine the accuracy of the measurement (see Appendix 1). The error is the further cooling that would have occurred during a period equal to the pulse duration added to the end of the cooling period, and thus the criterion for setting the duty cycle is to keep this virtual cooling to a minimum.

This method becomes more tedious with longer pulse durations if the transistor has a long temperature stabilisation time, and so a further modification is required. An initial indication of the temperature change is obtained quickly with some loss of accuracy, by using a duty cycle which does not fulfil the requirement. The operation then reverts to a measurement of the heating caused by a single pulse. However, with the indication obtained previously, the shift controls can be set approximately to the correct position before the pulse, and only minor adjustments need be made subsequently. The time during which the cooling is observed on the oscilloscope may be increased without loss of accuracy in the determination of the origin of cooling, because the cooling gradient is initially smaller after the longer heating pulses. The single transient may therefore be seen clearly.

The presence of spurious transients sometimes prevents the operation of the above methods with the required accuracy. The following adaptation may be used in these cases. First, the transient thermal resistance for a train of pulses is determined as in the previous section, and from this the required single-step response may be calculated using Eq.(8). To use this equation without the introduction of excessive error the duty cycle of the pulse train should be small enough to ensure that the values of $\theta_{t,d}$ and $\theta_{t,0}$ are similar. For example an accurate result will not be obtained if $\theta_{t,d} = 1$degC/W and $d\theta = 0{\cdot}99$degC/W.

The above and corresponding adaptations in the preceding section rely on a knowledge of the transient thermal resistance for a pulse duration t_2, the delay before the temperature is monitored. This may be obtained by extrapolation from provisional data for $\theta_{t,0}$, or by normalisation of results obtained with transistors free from spurious transients.

MEASURING APPARATUS

The measuring apparatus consists of two main parts. These are the power defining circuits which generate the rectangular power pulse trains, and the temperature measuring circuit. They are described below.

Power Defining Circuit

The basic circuit design is the same as that given in Ref. 6 with a few modifications (Fig. 8) to suit this application. The circuit incorporates emitter current switching to produce the fast edge necessary for accurate temperature monitoring.

The reference current, which also acts as a 'keep-alive' current for the emitter-base diode of the switching transistor TR_1, is defined by the voltage across the 'Set Reference Current' variable resistor R_1. During the temperature monitoring period, when the load current is cut off, the base of the switching transistor is caught at approximately +5V, thus defining the emitter voltage, and so, also, the reference current which flows into the emitter of the switching transistor. The corresponding collector current, which is the actual reference current to the transistor-under-test (t.u.t.) will remain constant provided that temperature effects, on the gain and V_{be}, of the switching transistor are negligible. A high temperature rise would occur in the switching transistor, if the maximum load current were passed continuously to the t.u.t. However, in general, this maximum current is only used for the shortest pulses, and the corresponding heating of the switching transistor is small. Further, stability of V_{be} variations is provided by the use of a comparatively high voltage rail for the reference current source.

The current generator TR_2 is a power transistor (OC23). The base of this transistor is taken to a potentiometer, R_2, which is the 'fine current control'. The emitter is connected through switched values of R_e, which is the 'coarse current control', to the +30V rail. The values of R_e and the available base voltage changes are such that the emitter current is continuously variable from 5 to 500mA. The small change in collector voltage which occurs when the current switches from the diode path to the switching transistor produces a negligible change in the corresponding collector current. Hence, irrespective of duty cycle, the d.c. meter in the collector indicates the pulsed current which flows into the switching transistor.

An important modification to the original circuit (Ref. 6) is the replacement of germanium switching transistor TR_1 (AUY10) by a silicon device with a much smaller leakage current. As a constant reference current is essential, any change in the junction temperature should produce a negligible change in the leakage current in comparison with the low reference current. Further, a high gain device

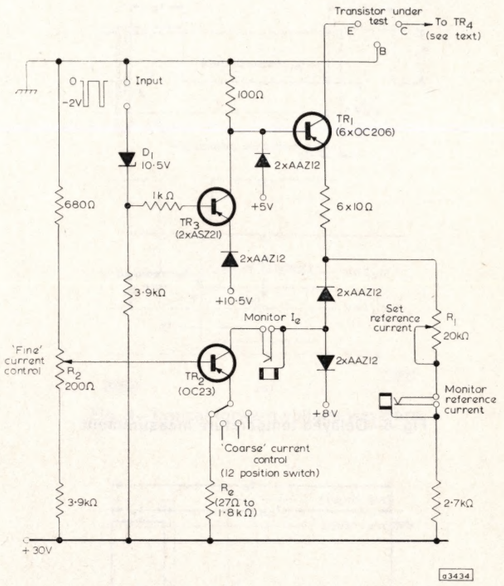


Fig. 8—Emitter current switching circuit

is required if the actual current, I_c, switched into the emitter of the t.u.t. is to be approximately equal to the nominal current, I_e, indicated by the meter. The fastest silicon p.n.p. transistor which meets the low leakage requirement and has reasonable gain is the OC206. The small power handling capacity of these devices limits the maximum load current: six devices on a common heatsink are used in parallel, with 10Ω emitter resistors to compensate for V_{be} differences.

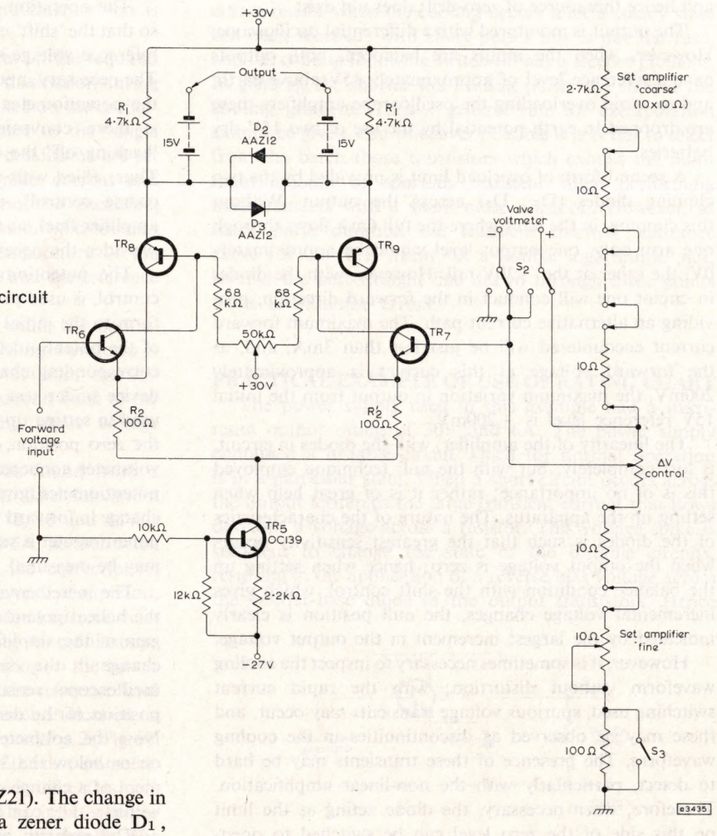
The collector supply voltage of the transistor under test is taken from the emitter of an OC24 (TR_4). This voltage may be varied in 6V steps from −6V to −24V by switching the position of the base between points along a chain of 6V zener diodes. For each voltage setting the collector resistor value is arranged such that the OC24 is just out of bottoming at the maximum current setting. This prevents excessive dissipation in the device so that even under steady state conditions the maximum temperature rise is limited to approximately 10degC.

Ignoring the slight variation of the collector supply voltage caused by the change in V_{be} of TR_4 with temperature, there is nevertheless a minor variation in this

voltage with load current. The small error in taking the nominal values may be eliminated by the use of a correction chart calibrated against load current. A similar correction chart can be used in determining the actual load current from that indicated by the meter.

With the measuring technique used, the base of the t.u.t. is at earth potential. Therefore it was necessary to displace the input signal level from the pulse generator to switch the driving transistors TR_3 (ASZ21). The change in d.c. levels is accomplished by using a zener diode D_1, in series with a resistor taken to the positive rail. The −2V signal is applied to the 'earthy' side of the diode and taken from the positive side.

Fig. 9—Amplifier and shift circuit



Temperature Measuring Circuit

The temperature measuring circuit consists mainly of a differential amplifier to give flexibility and good thermal stability. One arm of this amplifier is connected to the emitter of the t.u.t. to monitor its base-emitter voltage, and the other to a 'shift' voltage which is used as the backing-off facility.

Amplifier

The amplifier circuit (Fig. 9) is a modification of that described in Ref. 7. Briefly, the operation is as follows: the constant current source TR_5 from the negative rail demands that 6mA be provided by the two arms R_2 and R'_2. The two components of this current also flow through the emitter resistors R_1 and R'_1 in addition to the very small base currents of the n-p-n transistors TR_6 and TR_7, so that the ratio of the voltages across R_1 and R_2 is constant. The same occurs with R'_1 and R'_2. When the input voltages are such that the currents through both arms are identical then, if $R_1 = R'_1$ and $R_2 = R'_2$, there is zero output voltage.

We will now consider a change in the input, the base voltage of one arm, from this state. If this change has magnitude ΔV, the collector voltage of the constant current generator TR_5 will be changed by $\Delta V/2$, since the total current provided remains the same. Thus the changes in voltage across R_2 and R'_2 are $\pm\Delta V/2$, and the corresponding changes across R_1 and R'_1 are $\pm(R_1/R_2)\Delta V/2$. The total change of output voltage is $(R_1/R_2)\Delta V$; that is, the change in input voltage is amplified by the factor R_1/R_2 at the output.

The absolute voltage at the output terminals depends also on the forward voltages of the emitter-base diodes of the input transistors, and for the required temperature stability it is necessary to ensure that any thermal effects are

cancelled out. This is achieved by mounting the devices as closely together as possible on a large heatsink; any change in ambient temperature is assumed to produce equal changes in the forward voltages and therefore no effect on the current division.

The error due to variations in collector-base leakage current of the input transistors is kept very small by the use of silicon devices. The temperature sensitive parameter β does not appear in the formula for the output voltage, and hence this source of zero-drift does not exist.

The output is monitored with a differential oscilloscope. However, when the inputs are balanced, both outputs have a reference level of approximately 15V above earth, and to avoid overloading the oscilloscope amplifiers these are dropped to earth potential by the use of two 15V dry batteries.

A second form of overload limit is provided by the two clipping diodes (D_2, D_3) across the output. Without this clipping, in the limit where the full 6mA flows through one arm only, one output level would be approximately 0V, the other at the +30V rail. However, with the diodes in circuit one will conduct in the forward direction, providing an alternative current path. The maximum forward current encountered will be just less than 3mA, and, as the forward voltage at this current is approximately 200mV, the maximum variation in output from the initial 15V reference level is $\pm$200mV.

The linearity of the amplifier, with the diodes in circuit, is lost completely, but with the null technique employed this is of no importance; rather it is of great help when setting up the apparatus. The nature of the characteristics of the diodes is such that the greatest sensitivity occurs when the output voltage is zero; hence when setting up the balance condition with the shift control, which gives incremental voltage changes, the null position is clearly indicated by the largest increment in the output voltage.

However, it is sometimes necessary to inspect the cooling waveform without distortion; with the rapid current switching used, spurious voltage transients may occur, and these may be observed as discontinuities in the cooling waveform. The presence of these transients may be hard to detect, particularly with the non-linear amplification. Therefore, when necessary, the diode acting as the limit on this side of the zero level can be switched to open-circuit.

The Shift Circuit

In its simplest form the 'shift' or 'backing-off' circuit is a potential divider chain which is used to adjust the voltage at one input. However, since it is required to measure a small change in the forward voltage accurately, and this voltage differs considerably between different transistor types, good resolution must be obtained over a wide voltage range. This is achieved by switching a 10Ω helical potentiometer (ΔV control) between adjacent 10Ω resistors in a series chain. The current through the resistor chain is 10mA so that 100mV is dropped across each resistor and the potentiometer. With ten resistors in the chain the total variation possible at the input is 1·1V. This range may be increased to 2·1V by switching in a further 100Ω resistor to the negative end of the chain. Although it is unlikely that the forward voltage at the small measuring current level will exceed 1·1V, the extra range provides the facility for measuring the forward voltage during the power pulse so that an accurate assessment of the dissipation can be made. This may be relatively unimportant when testing transistors using a large collector voltage, but, for diodes, measurement of the forward voltage during dissipation is essential, and the forward voltage may well exceed 1·1V.

The operation of balancing the inputs of the amplifier so that the 'shift' input is made equal to that of the forward reference voltage will be termed 'setting up the amplifier'. The necessary input voltage could be defined by the use of the potentiometer and its positioning switch; however, it is more convenient to reserve the potentiometer for 'backing off' the waveform to the initial reference level. Thus, allied with the positioning switch (the set-amplifier coarse control), a separate 10Ω variable resistor (set-amplifier fine), at the negative end of the resistance chain, provides the necessary fine control required for balance.

The potentiometer, which provides a very fine shift control, is used to back off the origin of the cooling waveform to the initial reference level. The change in potential of the potentiometer slider gives a direct indication of the corresponding change in the forward voltage, ΔV, of the device under test. As the potentiometer is not normally used in setting up the amplifier, the slider may be kept at the zero position, so that, after backing off, a d.c. valve voltmeter connected across the more positive arm of the potentiometer, gives a direct reading of ΔV. With a typical change in forward voltage of −2mV/degC, the range of the potentiometer is such that a 50degC temperature excursion may be measured.

The incremental change in input which may be set by the helical potentiometer (the ΔV control) is 0·2mV. The gain of the amplifier ($\times$50) is such that a corresponding change in the output may be easily resolved with an oscilloscope sensitivity of 50mV/cm. Hence the null position of the displayed waveform can be set to 0·2mV. Now the voltmeter scale may be read to within 0·2mV on or below the 30mV f.s.d. range, so that the measurement of a change of forward voltage of 20mV accurate to within $\pm$1% can be made.

The polarity of the change in forward voltage with increased temperature requires that the potentiometer slider be brought nearer to earth potential when backing off. Hence, at the start of a measurement, the zero position of the slider should be at least 100mV above earth to allow the amplifier to be set up without the ΔV control. In order to produce a voltage-temperature calibration figure which is constant over a reasonably large temperature range, the ratio of the forward reference current to the reverse saturation current at room temperature should, as a general rule, be between 10^2 and 10^3. This will generally ensure that the forward voltage is far greater than 100mV. In practice only a limited temperature excursion is encountered in pulse measurement, and a forward voltage of 100mV is usually associated with a sufficient temperature range. Thus a satisfactory criterion in setting the reference current is that the forward voltage should be greater than 100mV.

OPERATION OF THE APPARATUS

The pulse generator is first set to give a constant −2V output so that no load current flows through the test device; that is, single cycle, positive. The constant measuring current is then adjusted to give a forward voltage greater than 100mV, and the amplifier is set up to give zero output, using both diode limiters and keeping the ΔV control turned down to minimum. By using the oscilloscope 'Y' shift controls, the output voltage waveform is positioned on a convenient line on the graticule, which is used as the reference level.

The pulse generator is then used to set up the required timing conditions, using a small value of dissipation during the 'on' time. The timing should be checked on the oscilloscope. After returning the pulse generator to the 'single cycle' position, the current and voltage conditions are set up. It must be noted that the maximum current and voltage ratings of the t.u.t. should not be exceeded, even though the temperature rise obtained indicates that more power could be handled. The temperature of the transistor should be allowed to stabilise and the reference level should then be checked.

After switching on the power pulse train, the oscilloscope is made to trigger so that the cooling waveform is displayed. When the waveform has stabilised, the ΔV control is adjusted to bring the initial portion back to the reference level, and the corresponding input voltage change is read from the valve voltmeter.

The collector supply voltage may be found from a chart calibrated against pulse current. The maximum correction to the nominal values of 6, 12, 18 and 24V is 0·2V at the maximum pulse current of 0·5A, so that when the larger collector voltages are used the correction is relatively insignificant. To obtain the overall dissipation, however, the base-emitter voltage under load current must be obtained. This is achieved by triggering the oscilloscope on that part of the waveform corresponding to the power pulse, and backing off the mean level to the reference level using the set amplifier controls. A direct indication is then provided by throwing switch S_2 into position 2 (Fig. 9).

Finally, the pulse current is read from the d.c. ammeter. As the circuit is using emitter current switching, this current is defined and flows in some part of the circuit whether the switching transistor is conducting or cutoff. The meter is so placed that the current flows in it through the whole period.

The above procedure will result in an indication of the change in the forward voltage per unit dissipation. To obtain the thermal resistance from this requires a calibration of the forward voltage change with temperature. For accurate results this should be carried out on the same measuring apparatus to eliminate indicator errors.

For measurements of the d = 0 curve, the approximation mentioned previously (see Appendix 1), may be used; the timing is set to give the correct pulse duration and a duty cycle such that during the 'off' time the rate of cooling is allowed to reach a small value. The set amplifier control is then adjusted so that the waveform at the end of the cooling time lies on the reference level. The trace is backed off by the ΔV control until the initial part of the cooling waveform lies on the reference level, and the voltage change indicated is read. This may be taken to correspond to the temperature rise caused by a single pulse of the same magnitude as those used in the measurement.

It is sometimes necessary to inspect the cooling waveform without distortion to determine the point at which the waveform is free of spurious ringing. If this occurs a considerable time after switch-off some sort of extrapolation should be used. Parabolic extrapolation only gives accurate results when the cooling occurs after a steady state has been reached; with short pulses this is not the case, and the cooling following switch-off has a steeper gradient. In general, the shorter the heating pulses the steeper the cooling gradient. Thus a general rule for extrapolation cannot be given, and whenever possible it is better to select from the batch those transistors which exhibit the minimum amount of spurious transient when performing measurements with a small pulse duration. However, at small pulse duration the transient thermal resistance curve for d = 0 is linear on a double logarithmic plot, so that the best straight line drawn through these points tends to minimise errors.

PRACTICAL EXAMPLE OF USE OF RATING CHART

The power supply used in this example had a maximum output rating of 30V and 6A. The power supply contained a bistable circuit which for normal operation is in a particular state. When a short circuit occurs across the output terminals the large transient current that flows develops a voltage across a resistor. This voltage spike is sufficient to change the state of the bistable circuits, resulting in the application of a reverse bias voltage across the emitter-base diode of the output transistors. Hence

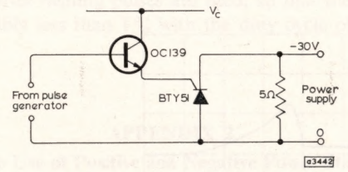


Fig. 10—Arrangement used to provide short-circuit (The BTY91-100R supersedes the BTY51)

the output transistors are cut off and the output current falls to zero. The bistable circuit, therefore, protects the output transistors and also the circuit being supplied by the power unit. On removal of the short circuit the bistable circuit can be reset and the power supply is again available for normal use.

Practical Results

The power supply was run at 30V and 6A and then an effective short circuit was applied across the output terminals using a thyristor, as shown in Fig. 10. The thyristor was triggered by single short pulses from a pulse generator; and the resulting waveforms, shown in Fig. 11, of collector

and emitter voltages and collector current of the six output transistors were obtained from photographs of the display from an oscilloscope. The power pulse in each device was obtained by taking the collector-emitter voltage and collector current from the photographs at specific time intervals and is shown in Fig. 12; the equivalent rectangle (see Appendix 3) is also shown.

Example 1

One of the conditions likely to occur is the short circuiting of the output. In the worst case this happens when the supply has been operating long enough to ensure that the output transistors have reached the maximum temperature indicated by the overall steady state thermal resistance. The waveform, modified so that the final pulse is rectangular, is shown in Fig. 13a.

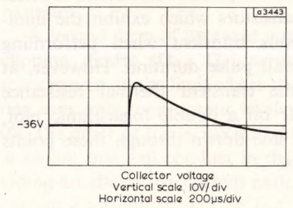
The output transistors used in the supply show a transient thermal response similar to that plotted in Fig. 14. From this we may ascertain that the transient thermal resistance of a single pulse of duration 300μs, thus, $\theta_{t,0}$, is 0·13degC/W, and that the steady state thermal resistance, θ_{j-mb}, is 2degC/W. The transistors are mounted on a heatsink for which $\theta_h+\theta_i$ is 1·8degC/W.

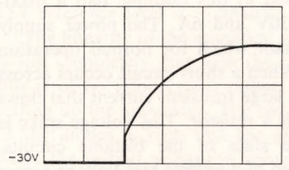
The temperature of the junction of one device is then given by

$$\begin{aligned} T_j &= T_{amb}+P\theta_{j-amb}+P_p\theta_{t,0} \\ &= T_{amb}+[6\times(2+1{\cdot}8)]+(55\times 0{\cdot}13) \\ &= (T_{amb}+30)°C\ . \end{aligned}$$

(Note that P_p is 55 watts (not 61) since the principle of superposition of power pulses requires that each power component must finish at the time when T_j is measured. Thus 6 watts of the short circuit pulse is regarded as forming the final part of the steady state component).

Thus if $T_{j(max)}$ is published as 90°C, the power supply can operate under the above condition in a maximum ambient of 60°C.





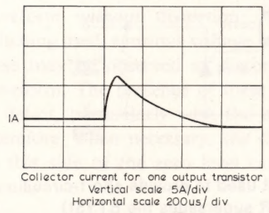


Fig. 11—Waveforms of current and voltage for the output transistors under short-circuit conditions

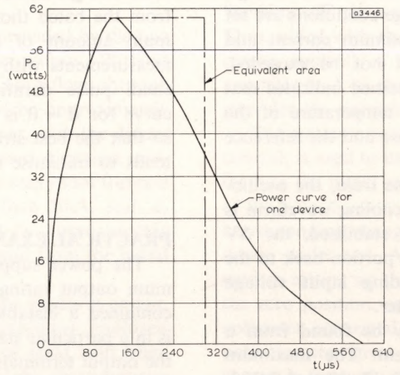


Fig. 12—Power dissipation in one output transistor under short-circuit conditions

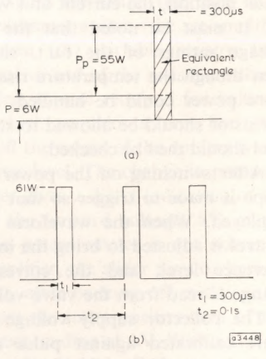


Fig. 13—Pulse-trains used in examples
(a) short-circuit load after long operation
(b) short-circuit load with supply being reset continuously

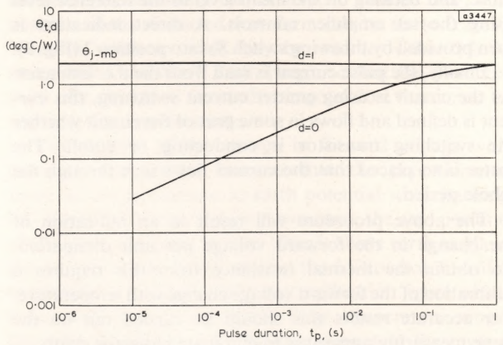


Fig. 14—Typical transient θ curve assumed for transistor used

Example 2

Another possible condition is for the short circuit to be permanent, with the operator continually resetting the supply. It is to be assumed that the supply can be reset in 100ms, which, from experience, is very optimistic. The resulting waveform, with each pulse modified to the equivalent rectangle as before, is shown in Fig. 13b. This

train of pulses is dealt with as in case 1 (page 148), using Eq.(4), that is,

$$T_j = T_{amb}+P_p\,.\,\theta_{t,d}+d(\theta_h+\theta_i)\,.$$

To find $\theta_{t,d}$ we may use Eq.(8), that is

$$\theta_{t,d} = d(\theta_{j-mb}-\theta_{t,0})+\theta_{t,0}$$

where $d = t_1/t_2$.

Substituting, we have

$T_j = T_{amb}+P_p(1-d)\theta_{t,0}+dP_p\theta_{j-mb}$ (compare Eq.9)

$$= T_{amb}+61\,.\left(1-\frac{0{\cdot}0003}{0{\cdot}1}\right)\times 0{\cdot}13+\frac{0{\cdot}0003}{0{\cdot}1}61(2+1{\cdot}8)$$

$= (T_{amb}+8{\cdot}6)°C$.

Thus the power supply could operate in a maximum ambient temperature of 81·4°C to observe a 90°C limit for T_j.

In both of the above examples the transistor voltage and current ratings are observed, and it is also apparent that the junction temperature rating is observed for all normal ambient temperatures.

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APPENDIX 1

Error in the Determination of $\theta_{t,0}$ by the Pulse Method

When the equilibrium condition is reached the temperature at the end of the cooling periods will, in general, be elevated with respect to the ambient. Hence the heating which occurs during the power pulses (Fig. 7) is superimposed on a higher initial temperature than is the case with the single pulse method, and the corresponding rise in temperature is smaller because of the greater loss of heat. The virtual cooling may be taken, as a first approximation, to be the cooling that would have occurred during the time t_p had the power pulse been absent.

For the purpose of calculating this error, the cooling curve may be regarded as a simple exponential of the form $A\exp(-t/\tau)$. The cooling during the time t_p at the end of a period t_{off} is given by the expression

$$A\left[\exp\left(-\frac{t_{off}}{\tau}\right)-\exp\left(-\frac{t_{off}+t_p}{\tau}\right)\right].$$

The measured cooling (ΔV) is given by

$$\Delta V = A\left[1-\exp\left(-\frac{t_{off}}{\tau}\right)\right].$$

Hence the error in the measurement is

$$\frac{A\left[\exp\left(-\frac{t_{off}}{\tau}\right)-\exp\left(-\frac{t_{off}+t_p}{\tau}\right)\right]}{A\left[1-\exp\left(-\frac{t_{off}}{\tau}\right)+\exp\left(-\frac{t_{off}}{\tau}\right)-\exp\left(-\frac{t_{off}+t_p}{\tau}\right)\right]}$$

$$= \frac{\exp\left(\frac{t_p}{\tau}\right)-1}{\exp\left(\frac{t_{off}+t_p}{\tau}\right)-1}\,.$$

When t_p and t_{off} are very small this value of the error tends to

$$\frac{t_p}{t_p+t_{off}} = d\times 100\%\,,$$

and decreases for longer pulse durations. Hence for pulse durations below this period τ, the error is less than 1% if a duty cycle of 0·01 is used. For longer pulse durations the cooling periods may be made relatively smaller until, in the limit where t_{off} approaches the temperature stabilisation time, the error becomes negligible.

The exponential decay was chosen for simplicity of calculation; in practice the cooling curves differ with pulse duration. Thus the 'time constant', τ, effectively decreases when shorter heating pulses are used, so that the error is considerably less than 1% with the duty cycle of 0·01.

APPENDIX 2

The Use of Positive and Negative Power Steps

As a positive step of power will produce heating of the junction, so will a negative step demand the cooling of the junction. The transient thermal resistance remains the same for both positive and negative power; thus, for example, if two power steps which are equal in magnitude but opposite in sign are applied to the junction simultaneously, the change in temperature with time will be zero. However, if the negative step is applied a time t_p after the positive step, the resulting temperature response is the same as that for a single pulse of duration t_p. By application of further positive and negative power steps at the correct intervals a train of pulses is simulated, and with the knowledge of the transient thermal resistance the maximum temperature in the equilibrium state may be calculated as the algebraic sum of the temperature responses of each step.

In general the number of pulses before equilibrium is attained is large and renders the above method unsuitable.

A good approximation is obtained as follows (Fig. 15a). Suppose the pulse train to have been applied long enough to allow the junction response to have reached the equilibrium state. The temperature with which we are concerned is that at the end of any further pulses. Let us first take the average of all the previous pulses to obtain a steady dissipation $d.P_p$. The pulse train may be simulated, to a first approximation, with respect to the maximum temperature only, by this steady power $d.P_p$ followed by a single pulse of power P_p. This may be thought of as a steady power level $d.P_p$ with a pulse of power $(1-d).P_p$, and the pulse component is $(1-d).P_p.\theta_{t_p,0}$. This leads to the following equation, comparable with Eq.(8),

$$\frac{T_j}{P_p} = \theta_{t_p,d} = d.\theta+(1-d)\theta_{t_p,0}. \qquad \ldots(16)$$

A closer approximation is obtained by following the steady dissipation $d.P_p$ with two power pulses (Figs. 15b and 15c). The equation which is obtained is Eq.(2), that is,

$$\theta_{t_p,d} = d.\theta+(1-d)\theta_{(t_r+t_p),0}-\theta_{t_r,0}+\theta_{t_p,0} \quad \ldots(17)$$

where t_r is the repetition period. The first term is caused by the steady dissipation taken as far as the end of the second pulse. (All power steps must be taken this far.) The second term accounts for the power $(1-d)P_p$ between the start of the first pulse and the end of the second, a period t_r+t_p. The third term accounts for the excess power after the end of the first pulse; that is, a negative pulse of duration t_r. The last term accounts for the second pulse.

The difference between the two above expressions for $\theta_{t_p,d}$ is given by

$$\Delta\theta_{t_p,d} = \theta_{t_r}-(1-d)\theta_{(t_r+t_p),0}-d.\theta_{t_p,0}. \quad \ldots(18)$$

For low pulse durations a parabolic relationship exists between $\theta_{t,0}$ and t. Thus, we may write

$$\frac{\theta_{t_1,0}}{\theta_{t_2.0}} = \left(\frac{t_1}{t_2}\right)^{\frac{1}{2}}. \qquad \ldots(19)$$

Writing $\Delta\theta_{t_p,d}$ in terms of $\theta_{t_p,0}$ we obtain

$$\Delta\theta_{t_p,d} = \theta_{t_p,0}\left[\left(\frac{t_r}{t_p}\right)^{\frac{1}{2}}-(1-d)\left(\frac{t_r+t_p}{t_p}\right)^{\frac{1}{2}}-d\right]$$

$$= \theta_{t_p,0}.\left[d^{-\frac{1}{2}}-(1-d)\left(\frac{1}{d}+1\right)^{\frac{1}{2}}-d\right]$$

$$= \theta_{t_p\,0}.f(d). \qquad \ldots(20)$$

A table of values of f(d) is given below.

d	f(d)
0·5	0·048
0·3	0·073
0·2	0·077
0·15	0·082
0·1	0·077
0·05	0·068
0·01	0·015

The fractional error in $\theta_{t_p,d}$ is therefore

$$\frac{\Delta\theta_{t_p,d}}{\theta_{t_p,d}} = \frac{\theta_{t_p,0}f(d)}{d\theta+(1-d)\theta_{t_p,0}}. \qquad \ldots(21)$$

If the parabola is extended to intersect the steady state value θ at a time t′ we may write the error as

$$\frac{\Delta\theta_{t_p,d}}{\theta_{t_p,d}} = \frac{\theta_{t_p,0}.f(d)}{\theta_{t_p,0}\left[d\left(\frac{t'}{t_p}\right)^{\frac{1}{2}}+(1-d)\right]}$$

$$= \frac{f(d)}{d\left(\frac{t'}{t_p}\right)^{\frac{1}{2}}+(1-d)}. \qquad \ldots(22)$$

Let us consider the value $d = 0{\cdot}15$, corresponding to the maximum value of f(d) (0·082). For pulse durations

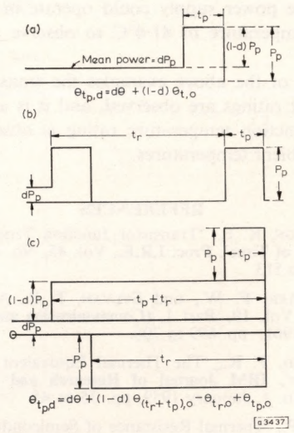

Fig. 15—Derivation of transient thermal resistance

shorter than t′/100 the error is less than 4%, falling as the square root of the pulse duration. For the longer pulse duration the error would appear to be greater when derived from the above formula. However, the parabolic nature of the $\theta_{t,0}$ curve does not in general extend this far in time, and higher power laws are necessary in the determination of f(d). These lead to correspondingly smaller values of f(d), and consequently involve smaller errors.

APPENDIX 3

The Thermal Response to a Train of Non-rectangular Pulses

The effective thermal resistance in the case of sawtooth and other non-rectangular waveforms may be determined approximately by the following treatment. Each pulse is modified to the rectangular pulse which has the same maximum power and total energy (Fig. 16). The new pulse duration and duty cycle may then be used to calculate the effective resistance or determine it from the chart.

The method is obviously an approximation, as can be seen from the following example. Consider two sawtooth waveforms, one having a fast rising edge, and the other being identical but reversed; that is, with slow rising and fast falling edges (Fig. 17). The above method will indicate the same maximum junction temperature for both operations; the effective thermal resistance will be $\theta/2$ for the

shorter equivalent pulses, rising to θ when the equivalent pulses are long. However, if both pulse trains are applied simultaneously to the device the total dissipation will be at a constant level, irrespective of the pulse duration, giving rise to a temperature change indicated by the value θ. Thus the sum of the effective thermal resistances for the two sawtooth waveforms is θ, so that the two components cannot be equal and greater than $\theta/2$ at the same time.

From the above we may conclude that the approximation holds good for the shorter equivalent pulses, since the

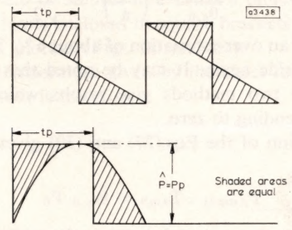

Fig. 16—Approximation for non-rectangular pulses

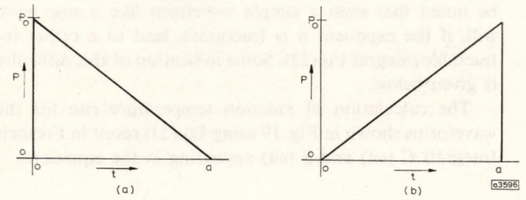

Fig. 17—First and second theoretical sawtooth waveforms considered

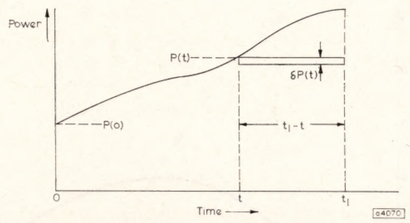

Fig. 18—Power-against-time waveform for single non-rectangular pulse

thermal capacitances surrounding the junction play a larger role in the smoothing out of the heat waves consequent on such pulses. This will be the case for any non-rectangular pulse train providing that the pulse duration is short enough. For the longer pulse durations the approximation may still be used but gives a larger safety factor.

APPENDIX 4

The Single Non-Rectangular Pulse

The following is an indication of a more exact treatment which may be applied to determine the temperature response consequent on a single non-rectangular power waveform. Comparison is made between the results of this method and the approximation of Appendix 3.

Consider the power waveform shown in Fig. 18 as a function of time.

This may be divided into horizontal strips of power of magnitude $\delta P(t)$. The temperature rise due to the typical increment shown is $\theta_{(t_1-t),0}\times\delta P(t)$. Using the principle of superposition of power steps (Appendix 2), the final temperature at time t_1 is given by:

$$T_j(t_1) = T_{amb}+\int_0^{P(t_1)}\theta_{(t_1-t),0}dP$$

$$= T_{amb}+P(0)\theta_{t_1,0}+\int_{P(0)}^{P(t_1)}\theta_{(t_1-t),0}dP$$

$$= T_{amb}+P(0)\theta_{t_1,0}+\int_0^{t_1}\theta_{(t_1-t),0}\frac{\partial P(t)}{\partial t}dt$$

(by using a 'dummy variable')

$$T_j(t_1) = T_{amb}+P(0)\theta_{t_1,0}-\int_0^{t_1}\frac{\theta_{t,0}\partial P_{(t_1-t)}}{\partial t}dt \quad \ldots(23)$$

Applying this to the sawtooth waveform of Fig. 17a, for which

$$P(t) = P(0)\left(1-\frac{t}{a}\right)$$

or

$$P(t_1-t) = P(0)\left(1-\frac{t_1-t}{a}\right)$$

we have

$$\frac{\partial P(t_1-t)}{\partial t} = \frac{P(0)}{a}. \qquad \ldots(24)$$

From examination of any of the pulse rating charts published, the $\theta_{t,0}$ curve appears as a straight line on a log-log plot, up to times approaching the stabilisation time.

Its equation therefore takes the form

$$\theta_{t,0} = At^n \qquad \ldots(25)$$

where n is found to range from about $\frac{1}{2}$ to 1.

Substituting Eq.(24) and Eq.(25) in Eq.(23)

$$T_j-T_{amb} = At_1^n.P_0-\int_0^{t_1}At^n\left(\frac{P_0}{a}\right).dt$$

$$= At_1^n.P_0-\frac{At_1^{n+1}.P_0}{a(n+1)} \qquad \ldots(26)$$

$$= \theta_{t_1,0}.P_0\left[1-\frac{t_1}{a(n+1)}\right]. \qquad \ldots(27)$$

Differentiation of Eq.(26) with respect to t_1 and equating the result to 0 gives the condition for T_j to be a maximum as

$$A.P_0.\left[nt_1^{n-1}-\frac{t_1^n}{a}\right] = 0. \qquad \ldots(28)$$

That is, T_j reaches a maximum value when

$$t_1 = na \qquad \ldots(29)$$

Assuming that n has the typical value $\frac{1}{2}$, substitution of Eq.(29) in Eq.(27) gives the maximum rise in T_j to be as follows:

$$T_{j(max)} - T_{amb} = \frac{2}{3}.\theta_{a/2,0}.P_0.$$

The usual approximation obtained by using the equivalent square wave pulse of duration a/2 and peak value P_0 would give

$$T_{j(max)} - T_{amb} = \theta_{a/2,0}.P_0.$$

This results in an over-estimation of the rise in junction temperature by 50%. This error is on the 'safe' side.

A similar analysis for the power waveform in Fig. 17b gives

$$T_j - T_{amb} = \frac{P_0 A t_1^{n+1}}{a(n+1)} = \theta_{t_1,0}.\frac{P_0 t_1}{a(n+1)}. \qquad \ldots(30)$$

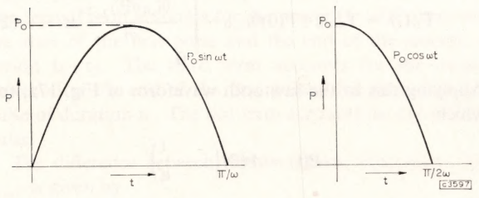

Fig. 19—Parts of sinusoidal waveforms considered

Substituting value $t_1 = a$ and $n = \frac{1}{2}$ in Eq.(30) gives

$$T_{j(max)} = \frac{2}{3}.\theta_{a,0}.P_0 + T_{amb}.$$

The equivalent square wave gives a value of $T_{j(max)}$.

$$T_{j(max)} = \theta_{a/2,0}.P_0 + T_{amb} = \frac{1}{\sqrt{2}}.\theta_{a,0}.P_0 + T_{amb}.$$

Since Eq.(25) gives

$$\frac{\theta_{a/2,0}}{\theta_{a,0}} = \left(\frac{a/2}{a}\right)^{\frac{1}{2}} = \frac{1}{\sqrt{2}}.$$

This gives an over-estimation of about 6%. The error is on the 'safe' side again. It may be noted that as n tends to unity, the two methods give results which differ by a quantity tending to zero.

The addition of the Eqs.(27) and (30) gives, for a square wave,

$$T_{j(max)} - T_{amb} = \theta_{t_1,0}.P_0.$$

This is to be expected, because the addition of the two power waveforms constitutes the step function P_0 (up to the time for which the formulae are valid).

The above serves as an illustration of the exact method to adopt for a non-rectangular waveform, but it should be noted that even a simple waveform like a sine wave will, if the exponent n is fractional, lead to a rather intractable integral Eq.(23). Some indication of this difficulty is given below.

The calculation of junction temperature rise for the waveforms shown in Fig. 19 using Eq.(23) result in Fresnels Integrals C (ωt) and S (ωt) appearing in the equations.

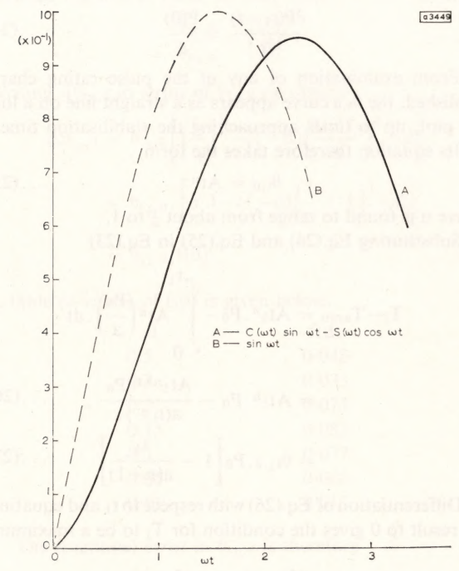

Fig. 20—Evaluated sine-cosine function in Eq.31

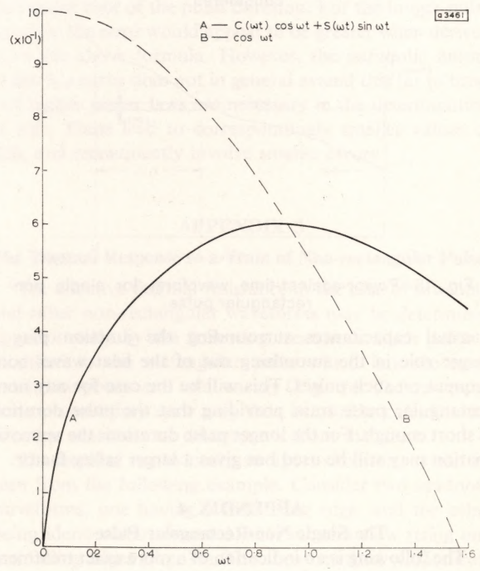

Fig. 21—Evaluated sine-cosine function in Eq.32

The expression for junction temperature rise for the half sine wave is

$$T_j - T_{amb} = P_0.\theta_{2/\omega,0}.\left(\frac{\pi}{4}\right)^{\frac{1}{2}}.[C(\omega t)\sin\omega t - S(\omega t)\cos\omega t] \qquad \ldots(31)$$

and for the quarter cosine wave,

$$T_j = P_0.\theta_{1/\omega,0}.\left(\frac{\pi}{2}\right)^{\frac{1}{2}}.[C(\omega t)\cos\omega t + S(\omega t)\sin\omega t]. \qquad \ldots(32)$$

With the help of Jahnke and Emde's tables of higher functions the terms enclosed in square brackets have been evaluated and plotted (Figs. 20 and 21).

The peak temperature given by the exact formulae for the half-sine wave is therefore

$$T_j = P_0.\theta_{2/\omega,0}.\left(\frac{\pi}{4}\right)^{\frac{1}{2}}0{\cdot}95 + T_{amb} = 0{\cdot}84P_0.\theta_{2/\omega,0} + T_{amb}. \qquad \ldots(33)$$

The square wave approximation results in a value of

$$T_j = P_0.\theta_{2/\omega,0} + T_{amb}. \qquad \ldots(34)$$

This is 20% over-estimation of the temperature rise.

In the case of the quarter cosine waves the peak temperature is

$$T_j = P_0.\theta_{1/\omega,0}.\left(\frac{\pi}{2}\right)^{\frac{1}{2}}.0{\cdot}6 + T_{amb} = 0{\cdot}75P_0.\theta_{1/\omega,0} + T_{amb}. \qquad \ldots(35)$$

The square wave approximation gives a value of

$$T_j = P_0.\theta_{1/\omega,0} + T_{amb}. \qquad \ldots(36)$$

This corresponds to a 33% over-estimation.

Cold Cathode Stepping Tube Multiple Store

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The principle of operation of a low-cost information store using decade stepping tubes, and in-line numerical read-out, is described. This system is intended for information storage and display in small business machines, machine tool control, and laboratory equipment.

The circuit design of a single-register store is also described in detail, and is followed by the method of adapting the circuit to form a multi-register store capable of operating at an input speed of 20kc/s.

An example of a three-register, twelve-decade multiple store for use in a desk calculator is given, together with the pulse drive and store selection arrangements. With this system, complete arithmetical operations take 60ms, which is considerably faster than the conventional electro-mechanical desk calculator, and it is noiseless in operation.

INTRODUCTION

Today there is a considerable potential market for systems of information storage and display in small business machines, machine tool control, and laboratory equipment. This article describes the principles and design of a cold-cathode stepping tube multiple store with in-line numerical readout. It is expected that with miniature low-cost stepping tubes, this solution offers real advantages over other storage systems in small 'computers' where cost reduction is of prime importance.

Since the whole design is based upon an information display technique called 'dynamic' display, the principle is described at the beginning of the article. The description is then separated into three sections as follows:

(i) A single stepping tube counter chain or 'register' using the dynamic mode of numerical display. (page 163)
(ii) The adaptation of this principle for more than one register – a 'multiple store'. (page 168)
(iii) The required programme and circuit details of a three-register, twelve-decade multiple store for use in a desk calculator, with the necessary pulse drive and gating arrangements. (page 172)

These sections are followed by a brief description of particular auxiliary circuits that may be used to complete the system.

PRINCIPLE OF DYNAMIC DISPLAY SYSTEM

Gasfilled numerical indicator tubes consist of ten cathodes shaped as numerals zero to nine, and one anode. A numeral glows when a current passes between the anode and that cathode. In conventional circuits, a required numeral is displayed by closing one of ten switches in the cathode leads. These cathode switches are usually operated by the ten positions of a decade counter. With this system, the cost of numerical indication increases in direct proportion to the number of numerical indicator tubes, as in each decade a complete set of ten cathode switches is required.

An alternative method of counting, storage, and display is now available which utilises one set of cathode switches for operating any number of tubes. This offers a substantial reduction in the cost of a system when four or more counting decades are necessary. This is termed the 'dynamic' drive for the numerical indicator tube. The block diagram for this method, shown in Fig. 1, consists of 'n' decade counters with carry facilities, and 'n' number tubes, with a common cathode switch unit. Each decade controls one anode switch for its corresponding indicator tube. The identical numerals are also commoned for all the tubes, and these are connected to the cathode switches. Finally, all the decades are driven from a single pulse generator. In principle, the anode and cathode switches can be any suitable electronic device.

Assume that the decade counter chain has counted a train of pulses and the count has ceased at 105, with the units, tens, and hundreds decades reading 5, 0, and 1 respectively. During the counting period, the cathode switches of the number tubes were open all the time, so that the display circuit was not operative. To display the stored information, the carry circuits are inhibited and pulses are applied to each decade counter simultaneously, so that all the decades are stepped in synchronism. In addition, the cathode switches are continually closed and opened in sequence, also in synchronism with the anode switch pulse generator.

To display the stored count, say '5' in the units decade, it is necessary to arrange that the anode switch of the units tube is always closed for the period that cathode switch number 5 is closed. Pulses of current will then flow into the tube via numeral 5 for one-tenth of the total cycle time, but no current will flow to any other numeral in the tube.

To illustrate the precise method of operation, Table 1 shows the events occurring in one ten-step cycle of the cathode switches, when the stored count is originally 105. At instant 'one' in the tube, the first pulse from the display pulse generator is applied to all decades, and the units decade in the example taken is stepped from position 5 to 6.

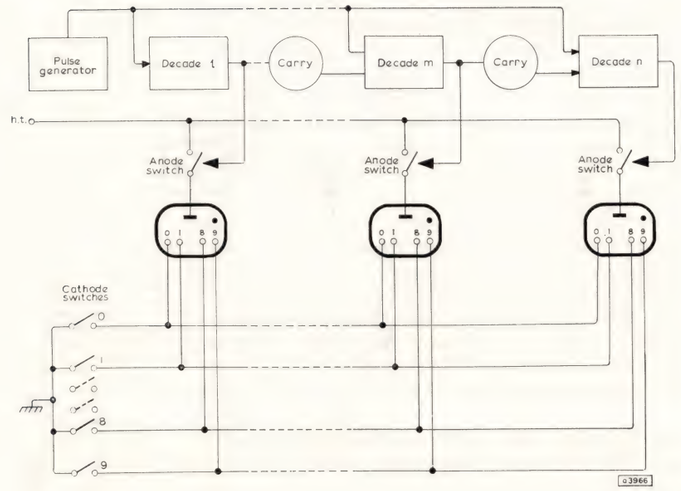


Fig. 1—Dynamic display system

TABLE 1
Example of Dynamic Display Operation

Time Interval	INSTANTANEOUS COUNT POSITION IN Hundreds Decade	Tens Decade	Units Decade	Cathode Switch Closed
Count to be displayed →	1	0	5	None
1	2	1	6	8
2	3	2	7	7
3	4	3	8	6
4	5	4	9→	→5
5	6	5	0	4
6	7	6	1	3
7	8	7	2	2
8	9→	8	3	→1
9	0	9→	4	→0
10	1	0	5	9

Simultaneously, cathode switch number 8 is closed. At instant 'two', the units decade steps from 6 to 7, the cathode switch number 7 is closed, and number 8 is reopened. In this manner, when cathode switch number 5 is closed, the units decade will have stepped to position 9. Further, after each subsequent set of ten time intervals, both the cathode switch and the decade counter will be in the same state: namely, at positions 5 and 9 respectively. Thus if the 9 output of the decade counter is arranged to close the anode switch of its corresponding number tube, then in this tube the numeral 5 only will pass current and glow.

Table 1 also shows the sequence of events for displaying the content of the other two decades on their corresponding number tubes. Because of the persistence of vision, an apparently continuous display showing number 105 is obtained when the switching speed is in excess of 500 steps per second. The current flow during the conduction period has to be approximately ten times greater than the normal direct current if the tube is to produce the same brightness in display.

Where it is desired to retain the count originally stored in the counter chain at the end of the display period, this is simply achieved by terminating the display period after an integral number of ten-pulse periods.

This system of display can in principle be employed with any form of decade counter and cathode switch. The following section describes circuits which utilise cold-cathode stepping tubes as decade counters. (Refs. 1, 2, 3, 4).

SINGLE STEPPING TUBE REGISTER WITH NUMERICAL DISPLAY

The circuit shown in Fig. 2 forms the basis of a multiple store. It consists of a series of stepping tubes connected as a decade counter chain, and driven from a common

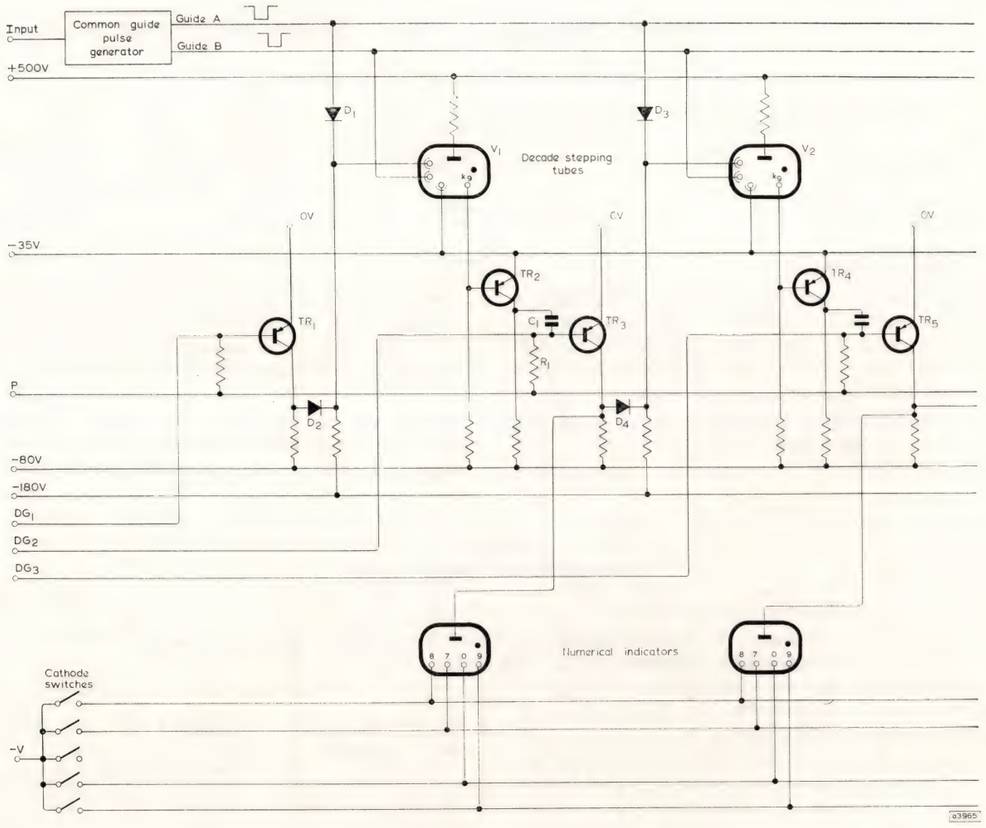


Fig. 2—Single stepping tube register with numerical display

guide pulse generator. Instead of re-generating the guide pulses for each stepping tube down the chain, the transistor circuits gate the common guide pulses to each tube as required.

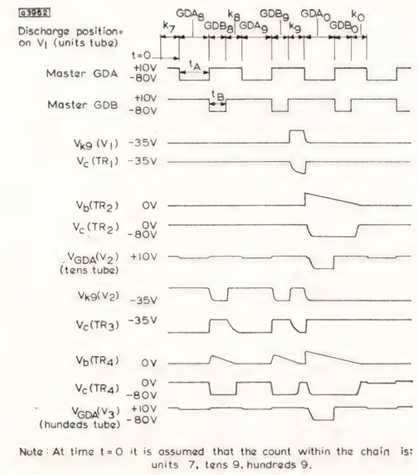
The transistor gates also control the anode current to a series of numerical indicator tubes, which are used as read-out indicators during the display period. The numerical indicators are connected between a negative line and the transistor gates via ten cathode switches. As only one set of ten cathode switches is required for all the numerical indicators, like numerals in the indicators are connected together, and returned to one cathode switch. The cathode switch may use either cold cathode tubes or semiconductors, and does not influence the fundamental action of the store.

CIRCUIT OPERATION AS A COUNTER

During counting, the negative guide B pulses are applied direct to each tube in the chain, but the negative guide A pulses are applied to the tubes via diode gates D_1 , D_2 and D_3 , D_4 etc., and the cathode switches are open so that the numerical indicators take no part in the process. In the absence of control signals at the terminals DG_1 , DG_2 , all the gating transistors TR_1 , TR_3 are conducting and bottomed so that the guide A cathodes are clamped at zero volts during the guide A period. With only attenuated guide A pulses applied to the tubes, no discharge is formed to the guide A cathodes, and the stepping mechanism is inhibited.

An input signal can be routed to any decade, simply by raising the potential of the gate control terminals, say DG_1 for the first decade, to a positive potential. Transistor TR_1 is then cut off, the guide A diode gate no longer clamps the guide A cathodes, and full negative guide A pulses may be applied to the tube.

A 'carry' signal for the next tube in the chain is obtained when the discharge steps off the k_9 cathode of the first tube. Fig. 3 shows the circuit waveforms during the carry process. As the discharge invests k_9 in the input decade, transistor TR_2 connected to k_9 is cut off and its collector potential falls toward the negative supply potential. The next guide A pulse steps the discharge off k_9 so that transistor TR_2 conducts again, and the positive pulse applied to the base of TR_3 switches this transistor off. The fall



Note: At time t = 0 it is assumed that the count within the chain is: units 7, tens 9, hundreds 9.

Fig. 3—Waveforms showing circuit operation during counting period

in collector potential of TR_3 to −80V coincides with the GDA pulse, applied to V_2 via diode D_3; and since the potential of the guide A electrode of tube V_2 is no longer clamped by diode D_4 , then a full GDA pulse is applied to V_2 . This pulse, followed by a guide B pulse, steps the discharge in V_2 to the next main cathode. The time-constant C_1R_1 is selected so that transistor TR_3 is cut off for the duration of the GDA pulse; but conducts, and is bottomed again, before the arrival of the next GDA pulse. The second decade, V_2 , therefore receives one guide A pulse for every ten guide A pulses applied to V_1 . Thus the second decade receives the tenth, twentieth, thirtieth, etc., GDA pulses. The third decade receives in the same manner the hundredth, two-hundredth, etc., GDA pulses.

The advantage of this 'gated circuit' counter is that information can be fed into any decade in the chain, simply by applying a d.c. signal to one of the control terminals, DG. For example, if a count of 1 000 000 is to be added into a counter chain, one pulse is added into the seventh decade, rather than a million pulses into the units decade.

In all stages, except the unit stage, ten or multiples of ten GDB pulses are applied in conjunction with attenuated GDA pulses; simultaneously the discharge in the previous tube invests the k_9 cathode. During these periods the discharge steps continuously between the main cathode and the preceding guide B electrode until a guide A pulse permits the discharge to transfer in the forward direction to the next main cathode. If the discharge is on k_9 , this continuous stepping back and forth to the preceding guide B cathode will continually open and close the gating circuit. Since, however, the gate is opened in coincidence with the GDB pulse, no signal can be present on the GDA line, and no undesired forward stepping of the discharge to GDA can occur.

INFORMATION DISPLAY

To display the information stored in the counter, the 'carry' circuits are inhibited, and full guide A and B pulses are applied to each stepping tube so that all the decades are stepped in synchronism. In addition, the cathode switches are opened and closed in sequence, from 9 to 1 and 0, also in synchronism with the guide pulse generator. The carry circuits are inhibited by changing the bias on line P from −80V to +10V. Transistors TR_1 , TR_3 etc., are then cut off, and full guide A pulses are applied to all the stepping tubes.

During display, the anode potential of each numerical indicator tube rests at −80V, except when the discharge in the corresponding stepping tube steps to k_9 . As the discharge steps to k_9 , for example in tube V_1 , transistor TR_2 connected to this cathode is cut off, transistor TR_3 conducts, and the anode voltage of the numerical indicator rises from −80V to zero volts for the duration of the k_9 rest period. When the next GDA pulse is applied, the discharge steps off k_9 , TR_2 again conducts, and TR_3 is cut off.

The cathode potential of the number tubes is arranged so that the number tube cannot conduct with an anode voltage of −80V, but will do so when the anode voltage is zero volts, and a particular cathode switch is closed. The numeral in the number tube to which conduction occurs will be determined by the position of the discharge in stepping tube V_1 at the start of the display period, as already described.

COUPLING CIRCUIT/ANODE SWITCH DESIGN

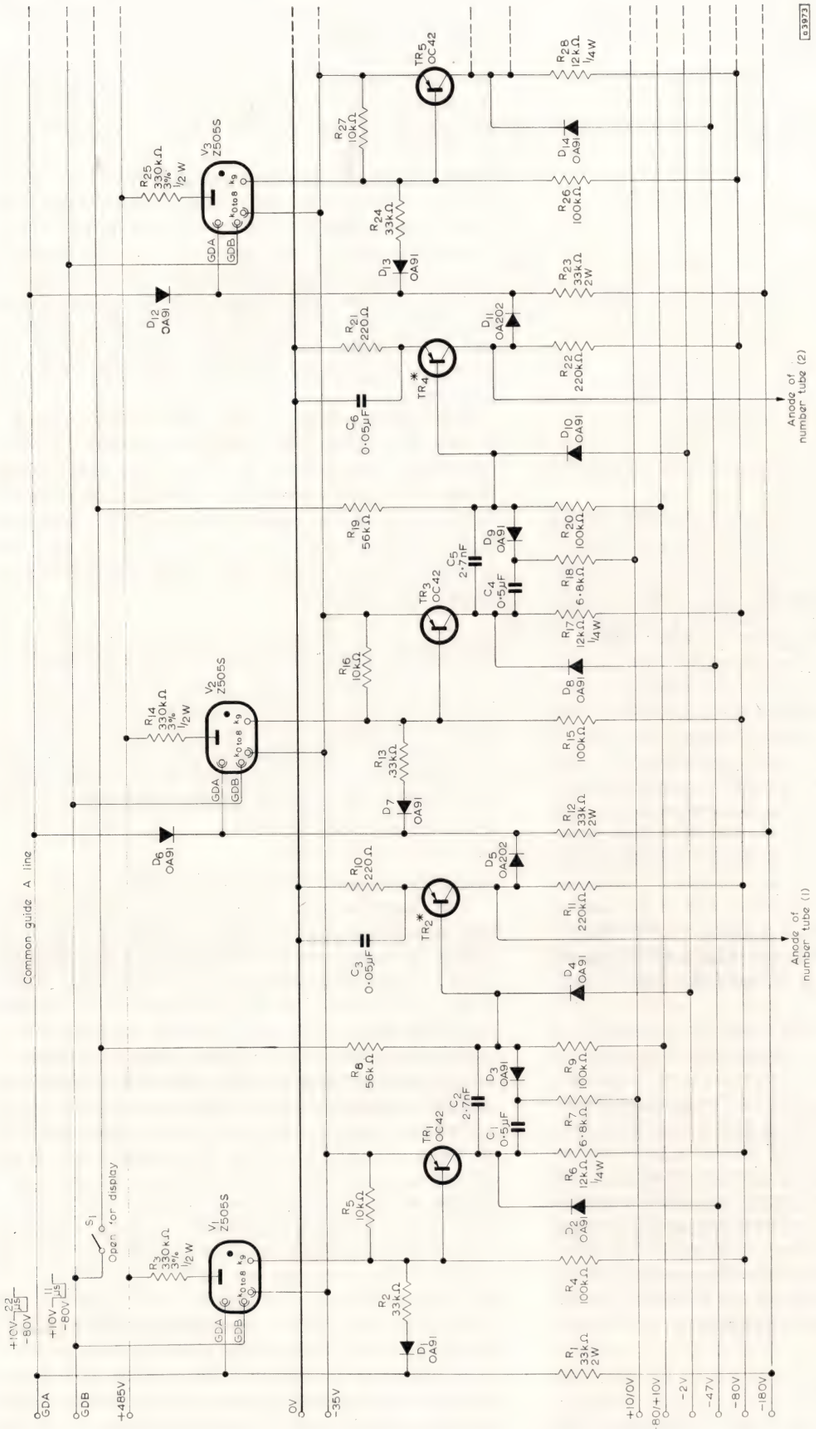
It is necessary to incorporate a number of additional features into the basic circuit discussed above in order to arrive at the optimal circuit shown in Fig. 4. Principally, these features are determined by two main requirements; the maximum input counting speed, and optimum display performance. The additions to the circuit are now discussed under these headings.

Circuit Requirements for Maximum Counting Speed

This circuit has been developed around a decade stepping tube which requires guide A, guide B, and main cathode discharge rest periods of at least 6μs each, defining a theoretical maximum operating speed slightly greater than 50kc/s. For the development of the circuit the Z505S stepping tube has been used. With this circuit configuration, however, it is not possible to achieve a circuit counting speed of 50kc/s owing to delays which occur in switching the transistor gating circuits.

Consider again the processes which occur when the discharge in tube V_1 (of Fig. 4) is stepped off the k_9 cathode by a guide A pulse. As this occurs, the flow of cathode current through R_4 stops, and the base potential of transistor TR_1 falls below its emitter potential. However, owing to the switch-on delay of the transistor, the collector voltage of TR_1 rises, and the transistor bottoms after a short delay. Similarly, the positive pulse applied to the base of transistor TR_2 via capacitor C_2 will only cut off TR_2 after the hole storage delay of the device.

The effect of these delays in opening the guide A gate of the succeeding stages is shown in Fig. 5, where it is seen that the guide A voltage falls at first only to the clamp level of transistor TR_2 ; and then, after the delay described,



*see page 168

Fig. 4—Complete coupling/anode switch circuit

All resistors are $\frac{1}{8}$W ± 10% unless otherwise specified
All capacitors are ± 10% 150V d. c. working unless otherwise specified

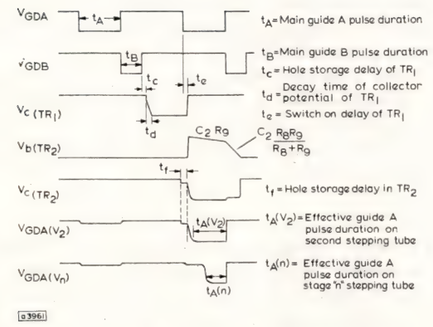


Fig. 5—Waveforms illustrating circuit delays during counting operation

the full pulse is applied. As this in effect delays the application of the guide A pulse to the second tube, the discharge in the second tube will leave k_9 after a similar delay. This in its turn produces a further equal delay in applying a guide A pulse to the third tube V_3. The effect can be seen as a cumulative delay down the counter chain, which corresponds to a decrease in guide A periods of rest, and therefore necessitates a proportionate increase in the guide A pulse duration with the number of decades. This corresponds to a reduction in maximum operating speed in order to preserve a GDA pulse of at least 6μs duration at the 'nth' tube in a counting chain of 'n' decades.

To minimise the switch-on delay of transistor TR_1, the components D_1 and R_2 have been added to the base circuit. These components provide a prepulse that switches on transistor TR_1 with the arrival of a guide A pulse on the common GDA line before the discharge steps off the k_9 cathode. The prepulse also reduces the base circuit resistance of TR_1 which permits it to bottom rapidly with a substantial collector current. Although the prepulse is applied to each decade in series, and any delay remains cumulative, the switch-on delay of the first transistor in each gating circuit is decreased by some 0·5μs.

It is also necessary to minimise the delaying effect of stray capacitance on the trailing edge of the guide A pulse, at the instant that TR_2 is cut off. This is achieved by returning the guide A cathode resistors R_1, R_{12}, etc., to a negative voltage, and then using the guide pulse generator to define the guide A pulse amplitude.

With these circuit additions the switching delay is reduced to approximately 1μs per gating circuit, most of this delay being the switch-on time for transistor TR_1, an OC42. With this value of switch-on time, the minimum guide A pulse duration required for a counter circuit of 'n' stages becomes (6+n)μs. With guide B and main cathode minimum rest periods of 6μs each, the theoretical maximum operating speed of the present circuit plotted as a function of the number of transistor coupling stages is shown as curve A–A in Fig. 6. However, when account is taken of ±10% pulse duration variations, the realistic maximum operating speed is shown plotted as curve B–B in the same figure.

The cumulative circuit delays impose certain additional requirements on the time for which capacitors C_2, C_5, etc., in Fig. 4 are required to hold transistors TR_2, TR_4, etc., cut off during the gating period. In the present circuit, a twelve-decade counter is designed for operation at a maximum speed of 20kc/s, and with a guide A pulse duration of 22μs. It is therefore necessary to ensure that capacitor C_2 in the first gating circuit holds TR_2 cut off for a minimum period of 22μs, and permits TR_2 to bottom again before 50μs have elapsed. In the last stage, however, owing to gating delays down the chain, the circuit is not activated until the first 12μs have elapsed, but must still switch on TR_{24} (the last transistor) before the next GDA pulse: that is, a time interval of 38μs. These two requirements are satisfied by returning resistor R_8 to the guide B line as shown in Fig. 4, so that when the guide B pulse is

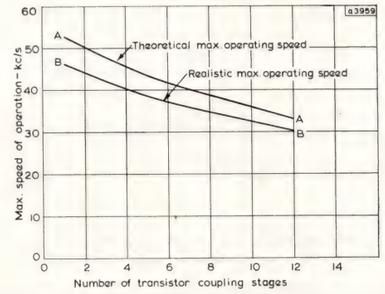


Fig. 6—Maximum operating speed vs number of coupling stages

applied, at the termination of the guide A pulse, the base circuit time-constant is modified from

$$C_2R_9 \text{ to } C_2.\frac{R_8.R_9}{R_8+R_9}.$$

Thus the guide B pulse acts as an impedance converter to speed up the recovery of the base waveform of transistor TR_2.

It is also worth noting that the collector load resistor of transistor TR_1 is returned to a large negative voltage and clamped by diode D_2. This reduces the collector fall-time, when TR_1 cuts off, to 6μs—the minimum main cathode period of rest. Finally, resistor R_5 is included to limit the reverse emitter-base voltage of transistor TR_1 to about 5V.

Circuit Requirements For Optimum Information Display

The circuit shown in Fig. 4 is intended to operate in the display mode at an input frequency of 2kc/s, corresponding to a main cathode rest period of 500μs. This is the maximum operating speed of the Z700U trigger tube cathode switches used in the application for which the store was designed.

During display, transistor TR_1 is cut off by the discharge to the k_9 cathode of the previous stepping tube. The current which then flows through the emitter-base junction of TR_2, capacitor C_2, and resistor R_6, should keep transistor TR_2 bottomed throughout the 500μs k_9 rest period. This requirement conflicts with counting operation, where the collector voltage of transistor TR_3 must fall to the diode clamp level in less than 6μs, and therefore necessitates an increase in the value of C_2. This is arranged as shown in Fig. 4, where C_1, D_3, and R_7, with the two switched

voltage levels, ensure that C_1 is parallelled across C_2 only during display operation. The practical waveforms in the circuit are shown in Fig. 7. The guide B drive pulses at R_8 are discontinued whilst in display by opening switch S_1, otherwise transistor TR_2 will conduct for short periods in the presence of the guide B pulses, and thus permit unwanted numerals in the number tube to display a faint glow.

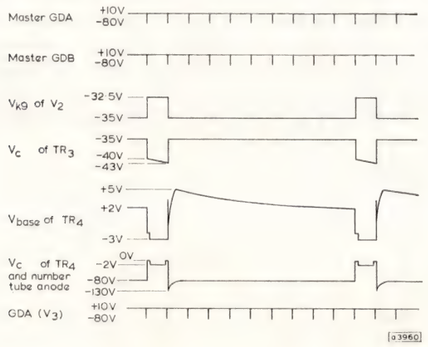


Fig. 7—Waveforms showing circuit operation during display period

A further requirement in the circuit is to define the anode current of the number tubes during display. A satisfactory level of illumination for numerical indicator tube ZM1080 is given with 10mA flowing for one-tenth of the total period at 2kc/s. This current is defined by the emitter resistor R_{10} in the circuit of TR_2 and the base clamp diode D_4. However, as the emitter of TR_2 is no longer a zero-impedance source, a guide A pulse arriving during normal counting may cause transistor TR_2 to come out of bottoming. This is prevented by making the emitter circuit of TR_2 a low-impedance current source by adding capacitor C_3 as shown.

Performance Requirements of Transistors TR_2, TR_4, etc

The circuit has been designed on the basis of a silicon transistor with the following main characteristic requirements:

Leakage current	$I_{co} \leqslant 5\mu A$ at T_{case} 50°C
Current gain	$h_{FE} \geqslant 15$
On-demand current gain	$\geqslant 12$
Collector-emitter voltage	$V_{ce} \geqslant -90V$
Emitter-base voltage	$V_{eb} \geqslant -100V$
Average collector current	$I_c \geqslant 10mA$
Total dissipation	$P_{tot} \geqslant 25mW$
Temperature operating range	T_{amb} 25 to 60°C.

CIRCUIT ADAPTATION FOR A MULTIPLE STORE

Where it is necessary to store, process, and display information in more than one store, for example in machine tool control and desk calculators, a number of stepping tube stores may be connected together to form a matrix. Any tube in this matrix may be selected for operation on 'cross-point' principles by applying both guide A 'column' and guide B 'line' pulses to the selected tube. Only one set of transistor coupling/anode switch circuits is necessary for operating the multiple store.

The three processes required in a multiple store are read-in, display of stored information, and the transfer of information from one store to another to perform arithmetic operations. These techniques are described in the following sections.

Read-in

The principle of operation is described with the aid of the simplified diagram of a multiple store shown in Fig. 8. Assume that input pulses are to be fed to tube 'm' in store II. It is necessary to close switch B_{II} to feed guide B pulses only to store II, and then select the column of tubes marked 'm' by switching off the transistor connected to the GDAm terminal in the transistor coupling gate. Then if a train of guide A and B pulses is produced at the pulse generator, tube m_{II} will receive both these pulses and the discharge in this tube will rotate.

It is also necessary to arrange a carry facility down the chain in store II between tubes m_{II} and n_{II}, n_{II} and o_{II} etc., as the stored number may exceed nine during read-in. This is simply achieved by connecting the k_9 cathodes of store II to the coupling circuit by taking this k_9 bias line to −35V. The k_9 bias lines of the other two stores are returned to −42V so that diodes D_4, D_6 remain cut off even when the discharge is resting on k_9 in these stores.

Thus when the discharge steps off k_9 in tube m_{II}, a guide A pulse is applied to the three tubes of decade n. The guide B pulse is, however, only applied to store II, so that the discharge is stepped to the next main cathode only in tube n_{II}.

Display

In order to display the information content of any store, the transistor gating circuit is switched to the anode switch function, and the discharges in the stepping tubes in each store are rotated continuously and in synchronism. The store to be displayed is then selected by raising its k_9 bias level to —35V so that only this store may operate the anode switch circuit. The inoperative stores are returned, as described in the preceding section, to a k_9 bias level of −42V. This arrangement has the major advantage that during display, which may occupy most of the operating time of a machine, all stepping tubes are rotated continuously, so that maximum life expectancy is assured.

The information content of all stores is retained by terminating the display after an integral number of ten-pulse periods.

Transfer

The content of one store is transferred to another by simultaneously reading-out the information from the first store and adding it to the second store without the need for an intermediate store. To transfer the contents of one tube in a store to another tube in a further store, a train of ten pulses is applied to the first tube, and the instant at which the discharge is stepped to k_0 is sensed. At this point in the process, the remainder of the ten pulses are applied to the second, or read-in, tube. For example, if

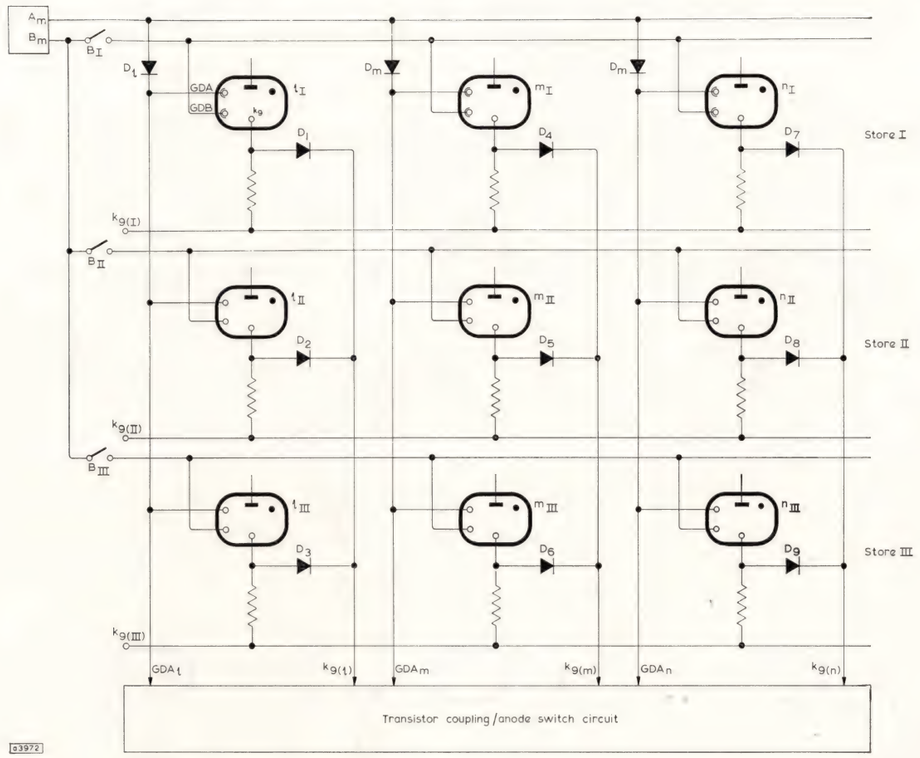


Fig. 8—Matrix selection of any tube in simplified multiple store

the content of the first tube is 7, then after three pulses the discharge steps to the k_0 cathode, and the remaining seven pulses are applied to the second tube, to register the count stored in the first tube. The stepping, of course, continues in the first tube to restore the count to its original value.

To examine the transfer process in more detail, assume that the content of tube 'a' in store I of Fig. 9 is to be added to the content of tube 'c' in store III.

First, it is necessary to connect the k_9 cathodes of store III to the transistor coupling circuit in order to obtain the read-in and carry function in this store. As it is not possible to use the guide A pulses from the Am supply to rotate the discharges in the tubes of store I, or to use this guide A supply for store III, an alternative set of switched guide A supplies is therefore introduced via the diode OR gates D_{15}, D_{18}, D_{16}, D_{19}, etc. These are shown in Fig. 9 as A_I, A_{II}, and A_{III}, and in this case A_I is connected to store I, so that ten pairs of pulses applied at A_I and B_I cause the discharge in all tubes of store I to make one complete rotation.

Finally, it is necessary to use a k_0 circuit exactly similar to that connected to the k_9 cathodes, so that by raising the k_0 bias level of store I to −35V an output is obtained from the k_0 cathode of the desired tube when the discharge invests k_0. Thus, in this example, when the discharge in tube a_I invests the k_0 cathode, the output voltage operates ancillary circuits to cut off the gating transistor for decade 'c' in the store. The gating signal is applied to the transistor by gate DG_3, which is shown in Fig. 10, and the remainder of the ten-pulse train is counted in the normal manner by tube 'c' in store III.

This process can be extended to transfer the information of all tubes in one store into a further store by sensing the k_0 cathodes of the read-out store in sequence, and selecting transistor gates DG in sequence, whilst applying a series of ten guide pulse waveforms to the read-out store.

Resetting a Store to Zero

There are two practical methods of resetting the discharge to zero in the multiple store. First a negative pulse greater than 100V may be applied to all the k_0 cathodes in a store to reset its content to zero. Alternatively, a lower value of negative bias may be applied to the k_0 bias line which is insufficient to reset all the tubes, When ten guide pulse pairs are then applied to this store, the discharge steps in all tubes to the k_0 cathode, but cannot step off k_0 because of its high negative bias.

The second approach is usually more economical for a desk calculator, since a ten-pulse source is readily available in decade systems, and the use of a negative bias of about 70V with respect to the other main cathodes permits inexpensive low-voltage diodes to be used in the k_0 circuit of each tube. These diodes are shown as D_{24}, D_{25}, D_{26} in decade 'b' of Fig. 9.

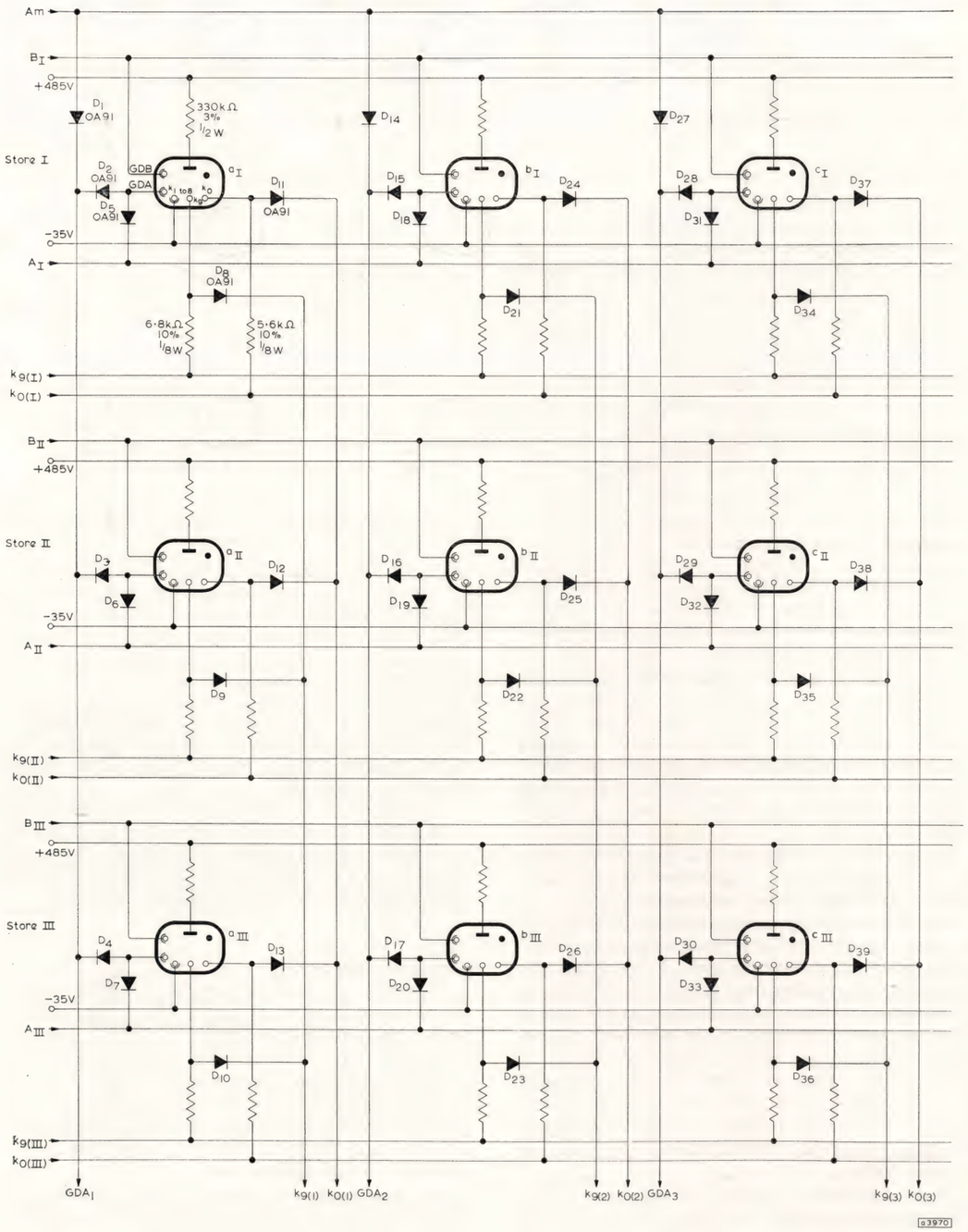


Fig. 9—Multiple store

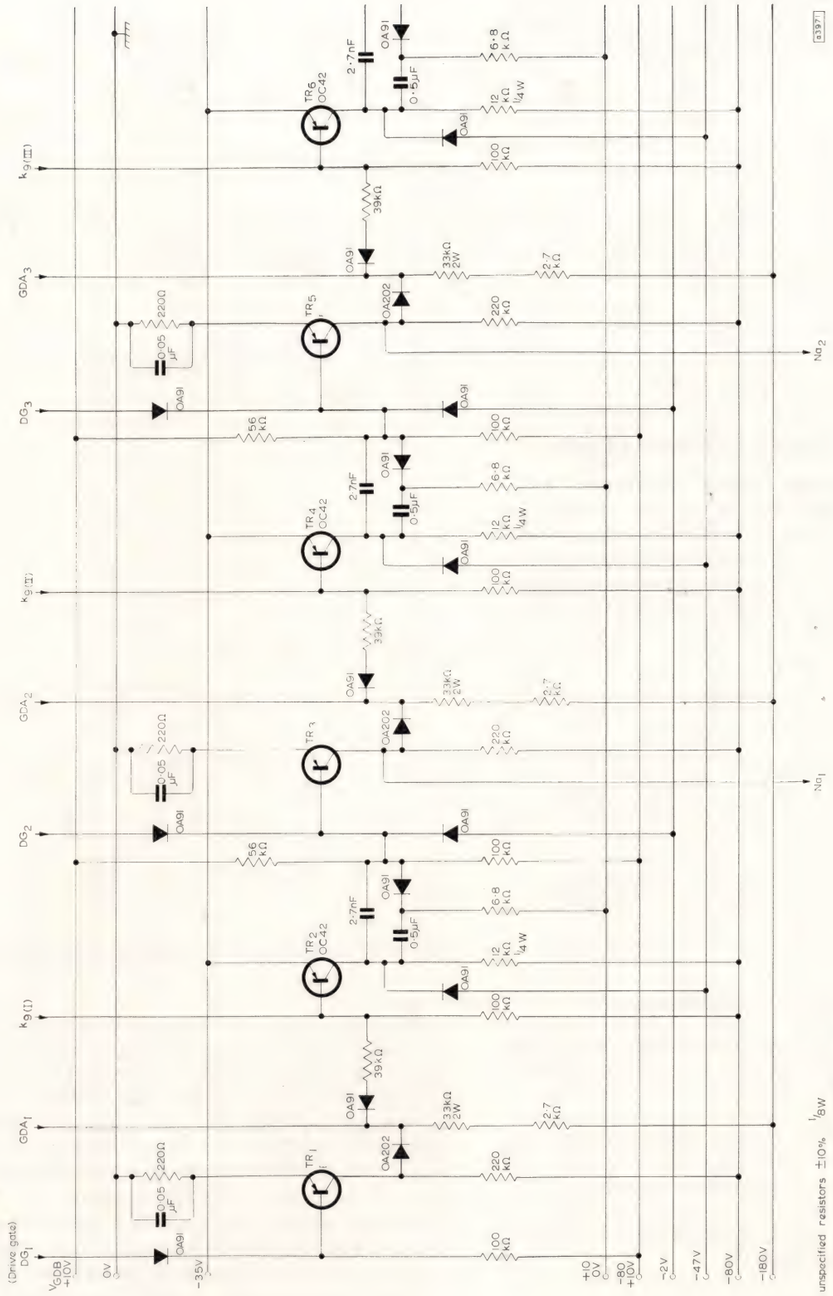


Fig. 10—Coupling/anode switch circuit for the multiple store

The transistor specification on page 168 applies also to TR_1, TR_3, and TR_5, in this circuit

PULSE DRIVE AND STORE SELECTION CIRCUIT FOR A PRACTICAL MULTIPLE STORE

Having described the principles of design and the circuit operation of a multiple store with in-line numerical display, it is useful to consider a particular system to illustrate typical examples of guide pulse drive and register selection circuits.

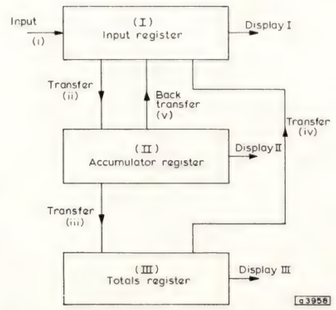


Fig. 11—Store programme for the desk calculator

Fig. 11 indicates the functions incorporated into a stepping tube multiple store for use in a Mullard desk calculator design* and Fig. 12 shows, in block diagram form, the complete circuit layout. Some simplifications of the circuit and connections result from the programmed requirements of this multiple store. For example, input information is only fed into register I.

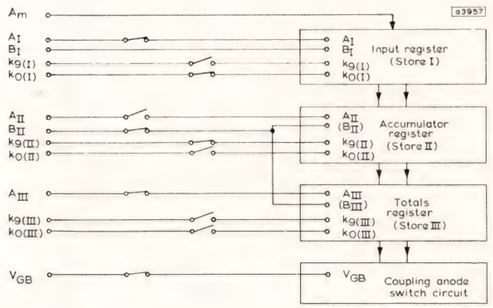


Fig. 12—Complete storage/display system

Table 2 (Page 174) gives k_9 and k_0 bias levels, and the pulse drive requirements for each of the required functions. This table is shown as a switching diagram in Fig. 13.

There is one guide B drive to stores II and III, since it is only necessary to switch off these drives when input information is read-in to store I. Interconnections between the k_9 and k_0 bias lines are also permissible in this programme, and these will be discussed under the heading *Store Selection Circuit* (page 174).

Guide Pulse Drive Circuits

Fig. 14 shows the guide pulse drive circuits used in the desk calculator multiple store, and Fig. 15 shows the drive circuit waveforms.

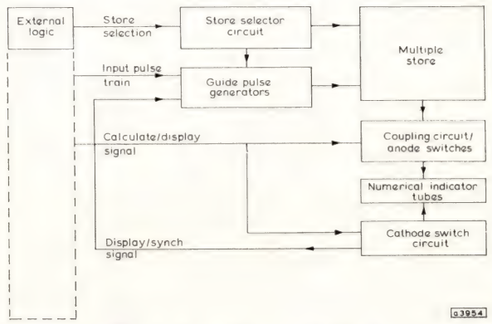


Fig. 13—Block diagram of Table 2

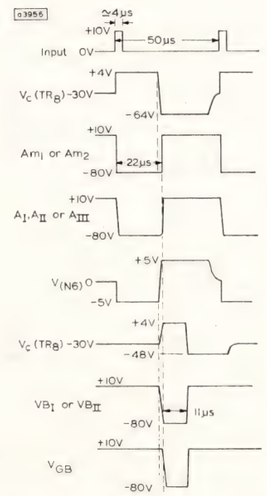


Fig. 15—Waveforms in the drive circuits of the multiple store

Blocking oscillator No. 1 generates a 22μs rectangular pulse when triggered by the input signal, and acts as the main guide A pulse generator. The output of this oscillator is amplified by transistors TR_3 and TR_4 for the high-current guide A lines Am_1 and Am_2. Slave amplifier transistors TR_5, TR_6, and TR_7 are also driven by the master guide A oscillator to produce the switched guide A signals A_I, A_{II}, and A_{III} for the three stores.

Blocking oscillator No. 2 acts in a similar manner to define the guide B pulse duration of 12μs. In this case, however, this master oscillator generates the guide B_I drive for store I directly from a secondary winding on the transformer.

Finally, amplifier TR_9, driven from blocking oscillator No. 2, generates the switched VG_B signal (see switch S_1 in Fig. 4,) for the transistor gating circuits, and the

*It should be noted that Mullard Ltd., do not manufacture or market this desk calculator.

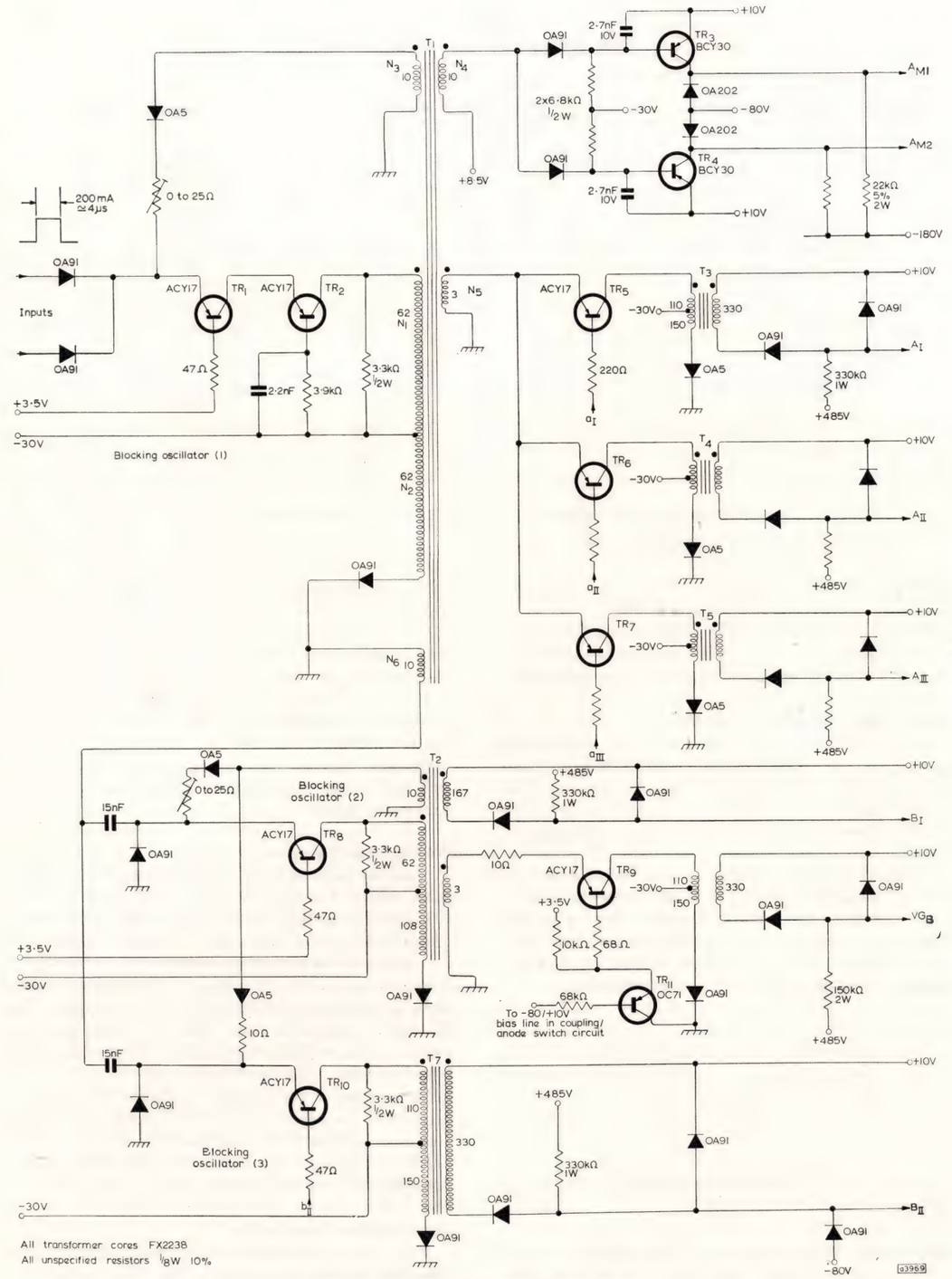


Fig. 14—Drive circuit for the multiple store
In transformers T_1 and T_2 the E-cores should be separated by a 7 μm gap

TABLE 2

Store Selection Logic for the Multiple Store

Condition	Store Operation	Main Cathode Bias Lines (on = −35V; off = −42V)						Guide Pulse Drive				
		$k_{9(I)}$	$k_{9(II)}$	$k_{9(III)}$	$k_{0(III)}$	$k_{0(I)}$	$k_{0(II)}$	A_I	A_{II}	A_{III}	B_{II}**	V_{GB}
1	Read-in Store I	on	off	off	—	—	—	off	—	—	off	on
1′	Display Store I	on	off	off	—	—	—	off	on	on	on	off
1	Transfer Store III to I	on	off	off	on	off	off	off	on	on	on	on
1′	Display Store I	on	off	off	—	—	—	off	on	on	on	off
2	Transfer Store I to II	off	on	off	off	on	off	on	off	on	on	on
2′	Display Store II	off	on	off	—	—	—	on	off	on	on	off
3	Transfer Store II to III	off	off	on	off	off	on	on	on	off	on	on
3′	Display Store III	off	off	on	—	—	—	on	on	off	on	off
4	Back Transfer Store II to I	on	off	off	off	off	on	off	on	on	on	on
4′ = 1′	Display Store I	on	off	off	—	—	—	off	on	on	on	off

Where dashes are shown, cathode bias level and guide pulse drive are unimportant.

**B_{II} drive is common to stores II and III.

further slave blocking oscillator No. 3 produces the switched guide B signal for stores I and II.

The design and operation of the type of blocking oscillator used in this system is described elsewhere (Ref.4). A number of circuit features are, however, discussed below.

Master Guide A Blocking Oscillator

As the desk calculator utilises a −30V high-current supply it has proved economical to design the pulse transformers around this supply voltage. In this case two ACY17 transistors are used in cascode to achieve the desired voltage ratings of ⩾65V at the expected dissipation levels.

A resistor has been inserted in the base circuit of transistor TR_1 to limit the forward diode current of the emitter-base junction to a safe value at the start of the conduction stroke. A capacitor is connected across the base resistor of TR_2 to supply the hole storage current required for rapid switch-off at the end of the conduction stroke.

Main Guide A Drive Am_1 and Am_2

A common-emitter configuration is chosen for the circuit, as the high quiescent load current is an embarrassment in a transformer-coupled amplifier.

The load is shared equally between the two transistor amplifiers TR_3 and TR_4. The base capacitors ensure that the transistors remain cut off for a short time after the input signal ceases, to provide a pulse overlap between the guide A and guide B waveforms.

Slave Guide A Pulse Amplifiers A_I, A_{II}, and A_{III}

This amplifier configuration is used as it is convenient to control the circuits with a 2V signal at the base terminals a_I, a_{II}, a_{III}.

The output pulse duration is defined mainly by the duration of the applied input signal. However, with no emitter resistor and a high value base resistor, the pulse duration at the outer terminals is slightly increased by hole storage effects. This has the advantage of extending the pulse overlap between the guide A and guide B pulses.

In all the transformer-driven amplifiers, a series diode is inserted in the output signal path to remove the unwanted positive voltage pulses which occur on the second stroke of the pulse transformers. The resistor, and the additional diode across the winding, clamp the output voltage at 10V during this period.

Guide B Pulse Generator

Blocking oscillator No. 2 is driven from the differentiated output of winding N_6 of blocking oscillator No. 1. This arrangement ensures that the guide B pulse commences with a minimum delay after the guide A pulse ends.

A second guide B blocking oscillator, No. 3, is required to drive a switched guide pulse line. To define the leading edges of this pulse, transistor TR_{10} is also triggered from the same signal. The pulse duration is obtained from master oscillator No. 2 by deriving the emitter voltage from the emitter winding of oscillator No. 2.

In addition, a further guide B pulse is required to operate the coupling circuits. In this case a pulse overlap between the guide A and this guide B pulse is unnecessary, and the circuit is driven simply from another output winding of the master guide B oscillator, No. 2.

Store Selection Circuit

The k_9 and k_0 cathode voltage levels, and the guide pulse requirements to perform each of the functions in the desk calculator multiple store, are given in Table 2. Most of these requirements fall conveniently into three groups, and the three-stage cold cathode trigger tube

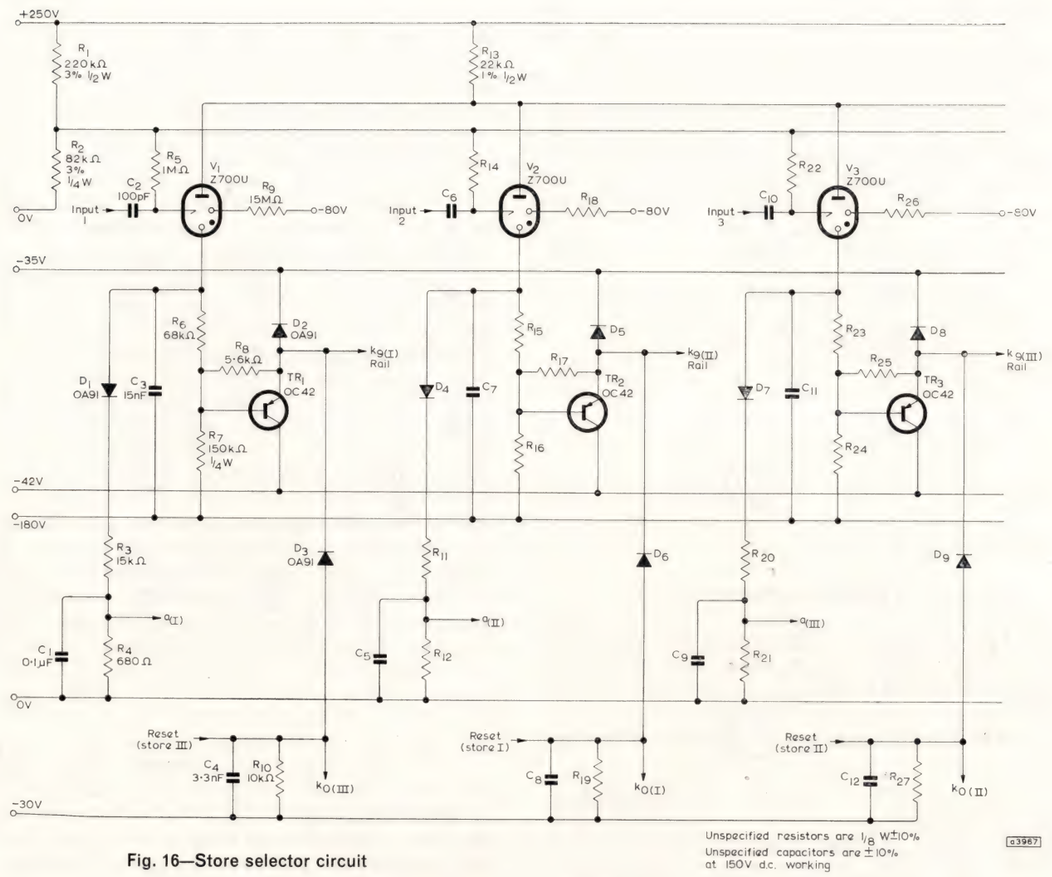


Fig. 16—Store selector circuit

circuit shown in Fig. 16 is used to perform the switching action. The circuit is arranged so that a command signal fires one trigger tube, and the ignition of that tube extinguishes the previous tube, so that only one tube conducts at any time.

With tube V_1 conducting, the potential divider R_6 and R_7 ensures that transistor TR_1 is cut off. Under these contions the emitter potential, and hence the potential of the k_9 cathodes of store I and the k_0 cathodes of store III, rest at −35V. In addition, the current flow through diode D_1 generates a voltage of approximately +2V at terminal a_I, the junction of R_3 and R_4, which is used to inhibit the guide A_I pulse amplifier in the blocking oscillator unit.

In the non-conducting stages, the transistor amplifiers in the cathode circuits of the tubes V_2 and V_3 are conducting and bottomed, so that the k_9 and k_0 cathode voltage levels rest at −42V. The bias levels a_{II} and a_{III} also rest at zero volts so that the guide A amplifiers A_{II} and A_{III} in the blocking oscillator unit are in operation.

To sum up, therefore, the three sets of programmed conditions depicted in Table 2, namely 1 and 1′, 2 and 2′, and 3 and 3′, are set up by igniting tubes V_1, V_2 and V_3 respectively in the store selection circuit of Fig. 16.

The back transfer shown as condition 4 and 4′ in the table may be achieved by using condition 1 and 1′, but reversing the connection of the $k_{0(III)}$ and $k_{0(II)}$ cathodes with an additional switch.

To complete the switching requirements, it is necessary to inhibit the guide B drive to stores II and III for at least nine input pulse periods when information is read-in to store I, and also to inhibit the guide B drive to V_{GB} during display, as shown in Fig. 14.

It is worth noting that a negative reset voltage may be applied to the k_0 cathode in any store without affecting the potential of the k_9 cathodes, since diodes D_3, D_6, D_9, etc., in Fig. 16 are reverse-biased during reset.

CATHODE SWITCH CIRCUIT FOR THE MULTIPLE STORE

Although the principles and design of a cold cathode stepping tube multiple store have been discussed in detail, no details have been given of cathode switches to drive the numerical indicator tubes. An example of a cold cathode trigger tube cathode switch is therefore given in Fig. 17.

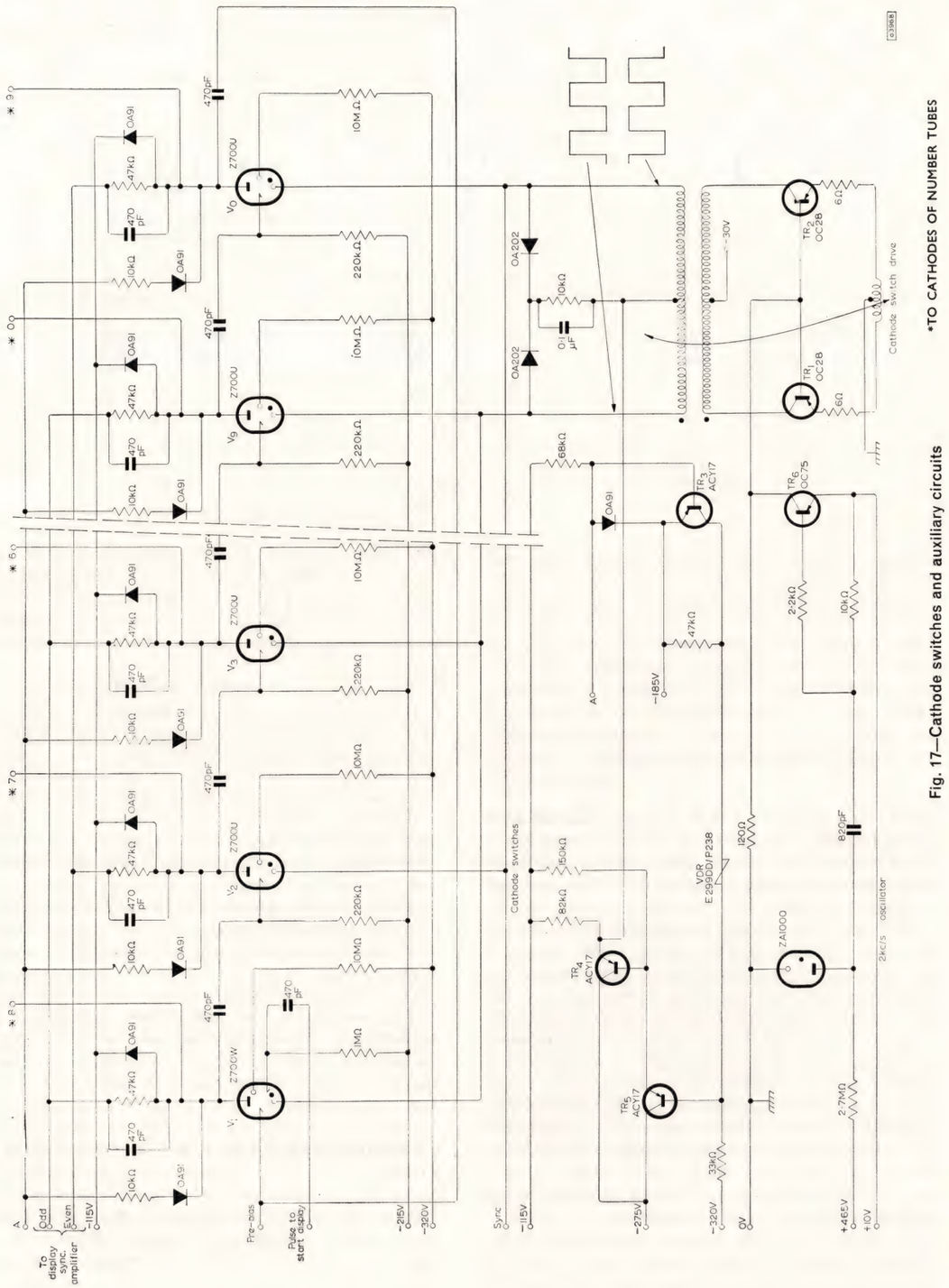


Fig. 17—Cathode switches and auxiliary circuits

The circuit employs ten trigger tubes in a ring counter, with the anode of each trigger tube connected to one cathode numeral of the number tubes. The ring counter is operated by applying square waveforms to the cathodes, a pre-bias to the trigger, and trigger pulses. A predetermined coincidence of these three signals steps the discharge in the ring counter, and hence closes and opens the switches in turn. The cathode waveforms are applied continuously and in antiphase to the odd and even cathodes.

When display is required, the operation of the ring counter is started by applying a starting pulse to trigger 2 of V_1. The starting pulse is synchronised with the application of the negative square waveform to the odd cathodes, so that V_1 ignites. The starting pulse will naturally only be applied after switching the required voltage levels in the coupling circuit to the anode switch levels. At the end of this half-cycle of the blocking oscillator, the positive potential of the waveform is applied to all odd cathodes, so that V_1 is extinguished. The resulting positive step at the anode of V_1 is applied via a coupling capacitor to the trigger of V_2. At this time a negative potential is applied to the cathodes of all even tubes, but only tube V_2 will ignite, since only this tube receives both a positive trigger pulse and a negative cathode voltage signal. After a further 500μs the blocking signal oscillator waveforms reverse again, so that tube V_2 is extinguished and tube V_3 is ignited in the manner described above. In addition to the trigger pulses, a continuous pre-bias is applied to the triggers of V_2 to V_0 and to trigger 2 of V_1. Trigger 1 of V_1 is pre-biased only when the circuit is in the display mode of operation. The latter pre-bias 'closes the ring' when tube V_0 extinguishes, and V_1 will ignite.

The cathode switches operate continuously while pre-bias is applied to the trigger of tube V_1. To switch the display off, the pre-bias is removed; so that when the discharge in the cathode switch ring counter reaches tube V_0, the output of V_0 is insufficient to ignite tube V_1, and the cathode switch operation ceases.

It is important to ensure that the cathode switches stop before the d.c. levels in the anode switch circuit are changed to the coupling circuit conditions, otherwise the information in the multiple store will be destroyed by applying fewer than ten pulses to the stepping tubes.

The cathode switch circuit is driven by a push-pull blocking oscillator which generates two 120V square waveforms.

The switching rate is controlled by a ZA1000 gas diode oscillator coupled to the base circuit of the blocking oscillator by an OC75 current amplifier. The free-running speed of the blocking oscillator is only 500c/s, but it is synchronised to 2kc/s by inhibiting the base current drive to the blocking oscillator transistors at a repetition rate of 2kc/s.

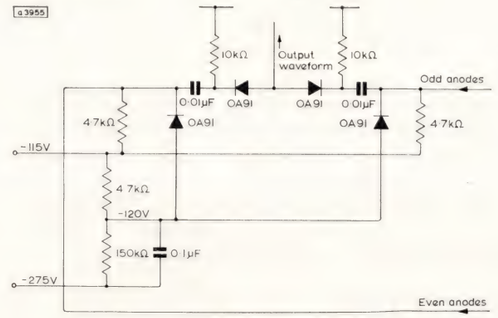


Fig. 18—Display synchronising amplifier

To drive the multiple store in synchronism with the cathode switches during display, output signals are obtained from the odd and even anodes of the trigger tubes by means of the circuit shown in Fig. 18, and these are used to drive the guide blocking oscillator system.

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Design of Field Output Stages for Television Receivers

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The design of practical field output stages for television receivers is described in this article. Particular emphasis is given to the design of the output transformer and to the wave-shaping required to produce a linear scanning current in the deflection coils.

The utilisation of the output valve, and the design of linearity correction circuits, are discussed in detail. A practical example of a complete timebase is given.

INTRODUCTION

The design of practical field output stages, consisting of conventional single-ended class A valve amplifiers which are transformer coupled to the deflection coils, is discussed. Particular emphasis is given to the design of the output transformer, since the transformer primary inductance has a major influence on the shape of the drive waveform required to produce a linear scanning current in the deflection coils. The utilisation of the output valve, and the design of the linearity correction circuits, are considered. A worked practical example of a complete timebase is given.

EFFECT OF THE OUTPUT TRANSFORMER PRIMARY INDUCTANCE

The calculation of the requirements of field output transformers has been covered previously (Refs. 1, 2 and 3). However, the theoretical calculations are repeated in a different manner to derive some necessary design equations (Appendix 1).

As the primary inductance of the transformer is reduced, the waveform of the anode current required for a linear scanning current is changed from a sawtooth (infinite inductance) to a parabola (which is caused by the finite magnetising current superimposed on the sawtooth current). The waveforms are shown in Fig. 1. The most common waveforms used are the zero initial slope (Z.I.S.), where the minimum of the parabola occurs at the start of scan; and the minimum mean anode current (M.M.A.C.) where the time at which the anode current waveform dips is chosen to minimise the average anode current. These waveforms represent theoretically defined modes of operation, but any intermediate mode is possible.

COMPARISON OF ZERO INITIAL SLOPE AND MINIMUM MEAN ANODE CURRENT DESIGNS

The main advantage of the M.M.A.C. design, is that a smaller and more economical transformer can be used. However, the drive waveform is more difficult to shape (perhaps requiring more components) and the effect of valve ageing has to be considered, because as the valve ages, the anode current decreases. With a Z.I.S. design, only the top portion of the raster would be cramped in the event of the valve being cut off at the start of the scan.

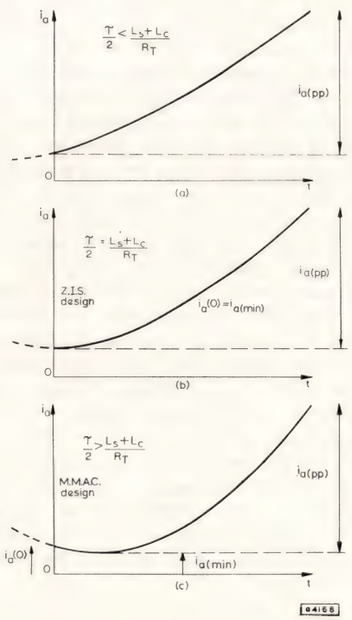


Fig. 1—Anode current waveforms

With an M.M.A.C. design, the raster would be cramped about one-third from the top, which would be more objectionable.

If the transformer peak magnetising current becomes a large proportion of the peak anode current, as in an M.M.A.C. design, it is possible that the non-linearity of the transformer inductance may cause non-linearity of scan. For this reason, the size of an M.M.A.C. transformer may have to be slightly larger than the theoretical minimum, to provide a more linear inductance. A similar increase in transformer size may be necessary with an M.M.A.C.

design if the transformer temperature rise is excessive because of the smaller surface area.

An advantage of the Z.I.S. design, is that the curvature of the $i_a - v_{g1}$ valve characteristic at low anode currents, helps to provide the s-correction of the scanning current required by modern wide-angle cathode ray tubes. This effect could not be utilised with an M.M.A.C. design.

In this article the Z.I.S. mode of operation is considered. The calculations for an M.M.A.C. design are covered in Ref. 1.

UTILISATION OF OUTPUT VALVE

The utilisation of the output valve depends on the design of the output transformer, because it is possible – within certain limits – to interchange the size of the output transformer and the output valve. Thus for a given scanning power in the deflection coils, a large output transformer may be used with a small output valve, or vice versa. The reason for this is that as the anode dissipation is increased, the peak anode current can be increased for a given h.t. voltage. The turns ratio is reduced, and hence the transformer primary voltage $V_p(\tau)$ is reduced. This means that a larger voltage can be dropped across the primary resistance, enabling more turns of a finer wire to be used; and since the required primary inductance ($L_p = n^2 L_s$) is also reduced, then a smaller core size can be adopted. It can be seen that the smallest and most economical transformer is obtained when the valve is used at its maximum anode dissipation. It is necessary that other factors such as the availability of the peak anode current, or linearity considerations, do not prevent the valve from being used at its maximum anode dissipation.

Anode Dissipation

Since the output valve is operating as a single-ended class A amplifier, the anode efficiency will be less than 50% and the anode dissipation will have to be greater than the power dissipated in the transformer and coils. An expression for the anode dissipation may be obtained from

$$p_a = \frac{1}{\tau}\int_0^{\tau} i_a v_a dt.$$

If expressions for $i_a(t)$ and $v_a(t)$ (Appendix 1) are substituted, this expression will contain terms of the form

$$\left(\frac{1}{2}\frac{L}{\tau}i^2\right),$$

which represents energy stored in the coils and transformer during scan. During flyback, this energy is dissipated in the valve, transformer and coils, and the proportion which is dissipated in the valve is difficult to ascertain.

Two limiting cases may be considered. First, the valve may be cut off during the flyback period so that the stored energy will have to be dissipated in the transformer and coils. This dissipation of energy could be achieved by inserting a resistor (5 to 10kΩ) in series with the oscillator charging capacitor (Fig. 13). The anode current in the triode discharges the capacitor, and causes a negative voltage pulse to occur across the resistor. The pulse is passed on to the grid of the output valve; thus it tends to cut the valve off during flyback.

The average anode dissipation of the valve may be reduced by approximately 0·5W by this method. However, a disadvantage is that the peak anode voltage is considerably increased, and external damping of the transformer may be necessary, which may be achieved by the use of a voltage dependent resistor or a resistor and capacitor in series across the primary of the transformer. A further disadvantage is that the linearity at the start of scan may be affected unless the flyback time is deliberately kept small.

The second case is to assume that all the stored energy is dissipated in the valve during flyback, which is not strictly accurate. However, it is shown later in this article that the output valve is the major damping element of the flyback voltage. For the purpose of design it is conservative to assume that all the flyback energy is dissipated in the valve. Therefore the anode dissipation is obtained by subtracting the energy dissipated in the coils, transformer and cathode resistance, from the total energy taken from the h.t. line; that is,

$$p_a = (\text{h.t.} - V_k)I_a - [i_{a(rms)}]^2 R_p - [i_{s(rms)}]^2 R_T - W_i ,$$

where

$i_{a(rms)}$ and $i_{s(rms)}$ are given by Eqs.(8, 9, 10) (Appendix 1), and the iron loss (W_i) is estimated later in this article. The anode dissipation should be calculated at the highest nominal h.t. voltage, using the values of the cold transformer resistances, since the transformer will take some time to heat up to its normal temperature.

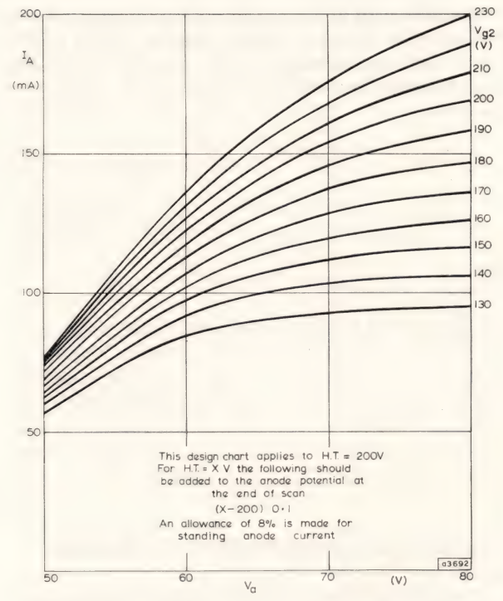


Fig. 2—PCL85 stabilised timebase design chart

Minimum Anode Potential at End of Scan

The anode potential at the end of scan should not be allowed to fall to such a value that the valve is bottomed, since this will cause severe cramping of the lower part of the raster. This condition should be avoided for low h.t. voltages, adverse component tolerances, and end-of-life conditions. The minimum end-of-scan voltage for a nominal valve at nominal h.t. voltage can be found from Fig. 2 for a PCL85 valve. The construction of this design chart is described in Ref. 4.

The total transformer voltage drop must be sufficiently low, so that the end-of-scan anode voltage does not fall below this minimum.

Standing Anode Current

In a similar manner, if the valve is cut off at low h.t. voltages under end-of-life conditions, then cramping of the top of the raster will occur. To avoid this possibility, it can be shown that a nominal valve at a nominal h.t. voltage should have a residual standing anode current at the start of scan. For a PCL85 output valve it is recommended that the standing anode current should be not less than 8% of the peak anode current. The design of the biasing circuit must be arranged to ensure that this minimum value of standing anode current is achieved.

OUTPUT TRANSFORMER DESIGN

The requirements of the output transformer are a specified primary inductance and turns ratio, with maximum permitted values of primary and secondary winding resistances. Because of the unidirectional anode current flowing through the primary winding, the operating cycle of the transformer core during scan is a minor hysteresis loop, fully contained in the first quadrant of the B-H loop which corresponds to the peak flux density at the operating frequency (Fig. 3). Since the field frequency of 50c/s is low, it is a valid approximation to say that the tips of the minor hysteresis loop will lie on the normal d.c. magnetisation curve.

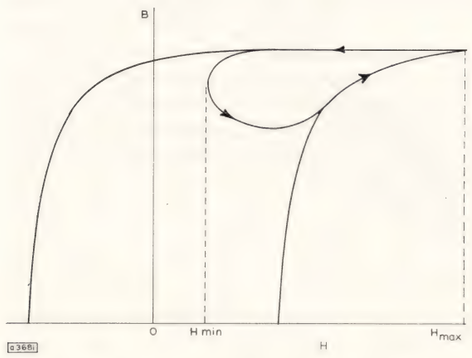


Fig. 3—Operating cycle of transformer core during scan

To minimise the size of the output transformer, the a.c. flux swing will be large (approximately 6000Gs) and the peak flux density will be near to saturation. It is necessary to prevent saturation by introducing an air gap in the magnetic path. The size of the air gap, the flux swing, and the anode current all influence the inductance, and to obtain a predictable design, the following method is used.

Sheared B-H Curve

The normal magnetisation curve for transformer iron is non-linear, with no simple formula for the relationship between B and H. Therefore, a graphical method of design is adopted (Ref. 5). Since there is a closed magnetic circuit consisting of an iron path (length ℓ_m) and an air gap (length ℓ_g): the total magnetomotive force = m.m.f. (iron H_i)+m.m.f. (air gap H_g)

$$\text{or } \frac{4\pi NI}{10} = \ell_m H_i + \ell_g H_g \text{ Gb}.$$

Dividing by ℓ_m,

$$\text{the total magnetising force} = \frac{4\pi NI}{\ell_m 10} = H_i + \frac{\ell_g}{\ell_m} H_g.$$

Now $H_i = f(B)$ for iron and $H_g = B$ for air. Therefore,

$$H_{(tot)} = f(B) + \frac{\ell_g}{\ell_m} B$$

It may be seen that the air gap can be represented on a B-H diagram by a straight line of slope ℓ_m/ℓ_g. If this line is plotted on the normal magnetisation curve for iron, the resultant magnetisation curve for the iron plus air gap combination is obtained by adding the curves from left to right (Fig. 4). The new operating cycle of the transformer core during scan is also displaced to the right. Its area is the same, because the iron loss is independent of the gap; but because the area is larger, its width is less. The effective, or average, permeability of the combination is taken as:

$$\mu_e = \frac{B_{max} - B_{min}}{H_{max} - H_{min}}.$$

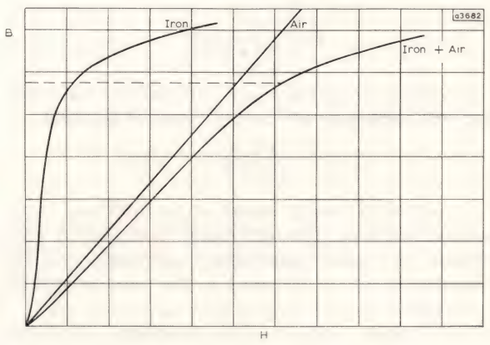
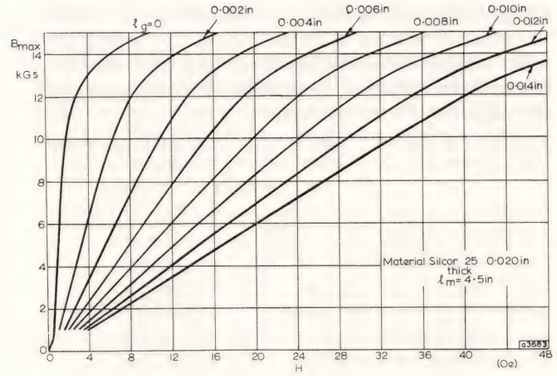


Fig. 4—Sheared B-H loop

The permeability, and hence the inductance, is non-linear, because of the curvature of the characteristic, but the non-linearity is reduced by the air gap. It has been

Fig. 5—Lamination pattern MEA35



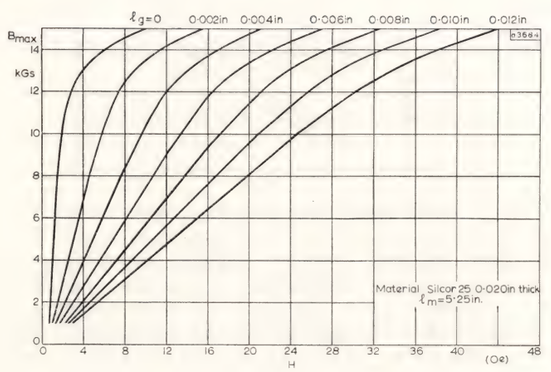


Fig. 6—Lamination pattern MEA147

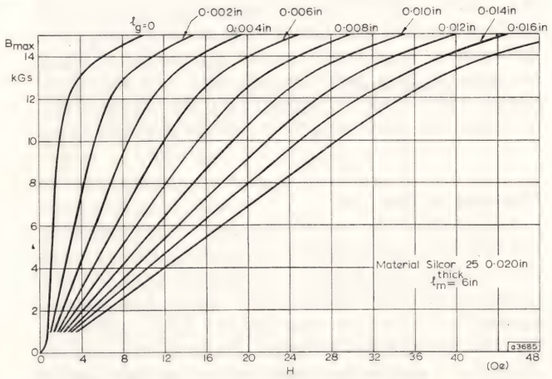


Fig. 7—Lamination pattern MEA29

confirmed experimentally that the non-linearity has no noticeable effect on the linearity of the scanning current, probably because in a Z.I.S. design the peak magnetising current is only about 20% of the peak anode current. Therefore, the average permeability is used for the purpose of calculating the inductance. It should be noted that for a given flux swing, there is an optimum value of air gap which increases the average permeability to a maximum. This occurs when the increase in average permeability, because of the reduction in polarisation of the iron, is compensated by the decrease caused by the higher reluctance of the magnetic path. The sheared B-H curves are drawn in Figs. 5, 6, 7 for several lamination shapes in common use. These are of the waste-free type as shown in Fig. 8. The material used is 0·4% silicon iron of 0·020 in. thickness. For this material, it was found that the optimum gap occurred when the peak flux density was about 13 000 gauss. There is no advantage in working at a higher flux density than that determined by the optimum air gap, since more turns are required, and the iron loss would be higher.

Calculation of Iron Loss

The transformer iron loss during scan is represented by the area of the minor hysteresis loop. During flyback, the existence of eddy currents in the transformer core should be taken into account. This loss is difficult to estimate because of the lack of available data. Consequently,

a crude estimate of the total iron loss is obtained by taking the difference in areas of the two normal hysteresis loops which correspond to the maximum and minimum flux density. This difference must be halved, since only the first quadrant is involved. (Fig. 3).

That is, iron loss = $\frac{1}{2}$ (loss at B_{max} − loss at B_{min}) W/lb.

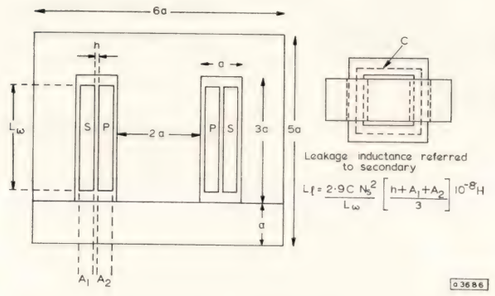


Fig. 8—Dimensions of waste-free laminations

MEA lamination number	35	147	29
Basic variable a (in)	$\frac{3}{8}$	$\frac{7}{16}$	$\frac{1}{2}$
Magnetic path length (in)	$4\frac{1}{2}$	$5\frac{1}{4}$	6

$\ell_m = 12a$

Although this method is not strictly correct, the correction to the anode current which it introduces (see next section) has been found by experiment to be of the correct order. The losses at B_{max} and B_{min}, for a frequency of 50c/s, are obtained from manufacturer's data, and are shown in Figs. 9 and 10 for the material used. The iron loss, W_i, is obtained by multiplying by the weight of laminations.

Allowance for Iron Loss

Fig. 11 shows the equivalent circuit of the transformer and deflection coils referred to the primary. It can be seen that the shunt loss current $I\ell$ flowing in R_o is supplied by the anode current ($i_{a(pp)}$, to be exact). This was not allowed for in the derivation of the Z.I.S. conditions. To allow for this loss in design, the turns ratio (Eq.(4), Appendix 1) can be increased in the proportion that the available $i_{a(pp)}$ is reduced by the shunt loss current. The shunt loss current may be estimated as follows.

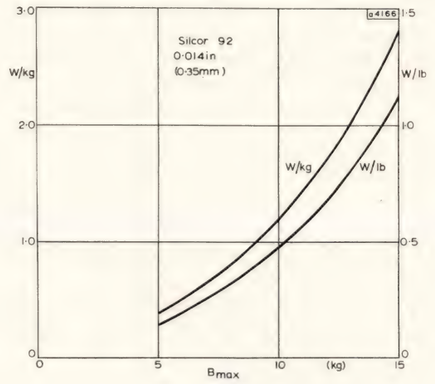
An iron loss of W_i watts is equivalent to a mean current of about $W_i/(h.t.-V_k)$ drawn from the h.t. supply. Because of the parabolic shape of the anode current waveform, this represents a peak-to-peak current of about $3W_i/(h.t.-V_k)$. Therefore, the peak-to-peak current available for calculating the turns ratio is,

$$i_{a(pp)}' = i_{a(pp)} - \frac{3W_i}{h.t.-V_k}.$$

The method of calculation gives a reasonably accurate result, especially when the iron loss is only a small fraction of the anode dissipation.

Transformer Primary Resistance

The transformer primary resistance has a maximum value determined by the minimum end-of-scan anode voltage calculated from Fig. 2. The maximum primary resistance should be calculated at the maximum transformer temperature. This value of resistance will depend



Figs. 9 & 10—Total iron losses

on the ambient temperature, and factors such as the ventilation and arrangement of components within the receiver.

The temperature coefficient of resistance of copper is 0·00393Ω/degC. If the temperature rise of the transformer above normal ambient temperature (say 20degC) is represented by ΔTdegC, then the maximum primary resistance is given by:

$$R_{p(hot)} = \frac{h.t._{(min)} - V_k - V_p(\tau) - V_{a(eos)}}{(1+0{\cdot}00393\Delta T)i_{a(pk)}}$$

where the values used correspond to $h.t._{(min)}$.

Temperature Rise

The maximum operating temperature of the transformer is usually limited by the insulating materials used in its construction. Materials commonly used for small transformers are paper, cotton, silk, varnish and standard wire enamel. These are classified as Class A materials, and the recommended maximum continuous operating temperature is 105°C, provided that the transformer is suitably impregnated. The use of synthetic enamel wires such as Lewmex or Lewcosol enables the maximum operating temperature to be raised to 120°C, but the insulation properties of paper interleaving cannot be relied on for continuous operation at this temperature. However, with synthetic enamel wires, the main function of the paper is to separate the layers and to prevent the possibility of two turns with a high voltage-difference from touching each other.

The transformer is also required to dissipate the power lost in the core and the power lost in the transformer winding resistances. The surface temperature of the transformer will rise until the rate of heat loss to the surroundings is equal to the rate at which it is generated internally. In addition, the interior of the transformer is hotter than the outside surface, with a temperature gradient existing across the windings. A method of calculating this temperature gradient is given in Ref. 6. For typical field output transformers, which generally have smaller losses than in the example quoted in Ref. 6, the maximum internal temperature is unlikely to be as high as 5degC above the surface temperature, and is approximately 2 to 3degC.

In view of these facts, it is recommended that 110°C is regarded as the upper limit for the maximum surface temperature. This limit enables the transformer to be impregnated in a high melting point wax such as Okerin 3700, which has a melting point of approximately 114°C.

A method of calculating the average surface temperature rise is given in Appendix 2.

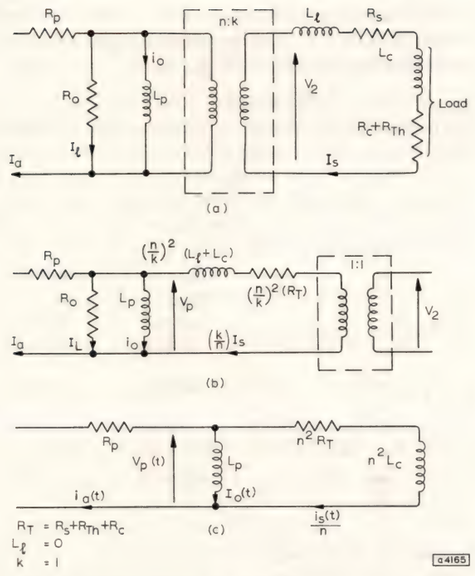


Fig. 11—Development of equivalent circuit on load

PRACTICAL EXAMPLE OF Z.I.S. TRANSFORMER DESIGN

In the following example, a PCL85 valve is used, with a maximum anode dissipation of 8W. The process of design may be conveniently divided into the following sections.

(1) Obtain the data on coils and h.t. line variations.
(2) Estimate the various losses in the transformer and coils at the maximum h.t.
(3) Calculate the sum of the maximum anode dissipation and the total losses, and calculate the valve bias resistances so that the anode dissipation under quiescent conditions is equal to this sum. Then under dynamic conditions the valve anode dissipation will be equal to its maximum rated value. The average anode current can be calculated, and its value at the minimum h.t. can be dimensioned to provide the necessary standing anode current and peak anode current.
(4) Calculate the transformer requirements such as inductance and turns ratio.
(5) Carry out the detailed transformer design.
(6) Calculate the transformer and coil losses and check the estimates in step 2.
(7) Repeat stages 3 to 6 as necessary.

Deflection Coils

The deflection coils to be used are the Plessey type TLA20240, catalogue number 413/1/00011/001. This refers to a field coil resistance of 38Ω, and an 8Ω thermistor is available. Another coil with the same resistance and similar inductance is type AT1011.

Inductance L_c = 89mH
Resistance R_c = 38Ω
Thermistor R_{Th} = 8Ω at 25°C (Mullard type VA1053)
Scanning current $I_{s(pp)}$ = 0·44A
E.H.T. = 18kV
C.R.T. = AW47–91
Vertical deflection = 30·4cm
Maximum h.t. = 240V
Minimum h.t. = 220V
Maximum anode dissipation = 8W at max. h.t.
Standing anode current = 8% of $i_{a(pk)}$ at min. h.t.
Flyback time = 1ms
Screen grid resistor (R_{g2}) = 0Ω

Estimate of Losses at Maximum h.t. Voltage

The peak-to-peak scanning current for 3% overscan at 18kV is 0·44 × 1·03 = 0·46A. Allowing for s-correction, this corresponds to an r.m.s. current of 0·142A. The total of the coil and thermistor resistance is 46Ω. It has been found that a transformer secondary resistance of about 25% of the coil plus thermistor resistance is a practical design value. Therefore, $R_s = 46 \times 0{\cdot}25 = 11{\cdot}5\Omega$ and $R_T = 57{\cdot}5\Omega$. The total secondary loss in the coil and transformer is $(0{\cdot}142)^2 \times 57{\cdot}5 = 1{\cdot}16$W. This is the only loss which can be calculated accurately at this stage. The primary copper loss is estimated at 1·5W and the iron loss is estimated at 0·5W. The sum of these losses is 3·2W, and for an anode dissipation of 8W, the valve has to be biased for a quiescent dissipation of 11·2W.

Bias Design

To calculate the value of cathode bias resistor, it is necessary to know the average cathode current. This current must be calculated under dynamic conditions, to allow for the increase in screen grid current with drive.

For the PCL85, a typical value of the $I_a:I_{g2}$ ratio under dynamic conditions is 7:1. For a quiescent anode dissipation of 11·2W at 240V h.t., the average anode current is

$$Ia = 11{\cdot}2/(240-V_k).$$

Hence, $I_k = \dfrac{11{\cdot}2}{(240-V_k)}\times\dfrac{8}{7} = \dfrac{12{\cdot}8}{(240-V_k)}$. By reference to Fig. 12 the bias point can be located using the condition that $V_{g2}+V_k = 240V$. This gives $I_k = 58{\cdot}2mA$ at $V_k = 20{\cdot}35V$, which means that R_k should be 350Ω. This can be achieved with a 360Ω 2W resistor in parallel with a 12kΩ resistor. If it is required to use a single preferred value for R_k, it is necessary to recalculate the bias point for $R_k = 360\Omega$, which results in an anode dissipation which is below 8W, and a larger transformer. With the value of R_k decided, the bias point can be located for the lower value of h.t., that is, 220V.

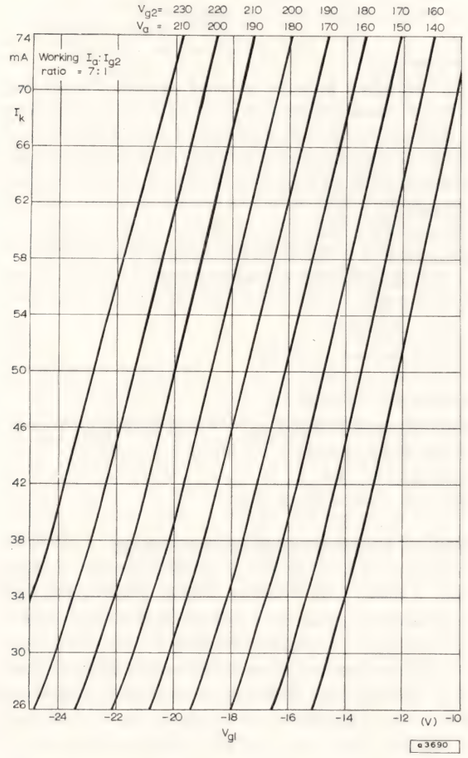


Fig. 12—PCL85 pentode nominal valve

For a standing anode current of 8% of the peak anode current at 220V h.t., it is necessary to make the standing anode current equal to 0·207 I_a, since

$$I_a = i_{a(0)}+\tfrac{1}{3}i_{a(pp)} = \tfrac{2}{3}i_{a(0)}+\tfrac{1}{3}i_{a(pk)}.$$

The peak anode current can be calculated, and the available peak-to-peak anode current obtained. The standing anode current and the peak anode current at $h.t._{(max)}$ are obtained by adding the increase in I_a to their values at $h.t._{(min)}$. The values of currents and voltages are summarised in the following table.

h.t.	220 V	240 V
V_{g2}	201·5V	219·65V
$V_k = -V_{g1}$	18·5V	20·35V
I_k	52·9mA	58·2mA
$I_a = \frac{7}{8}I_k$	46·2mA	50·9mA
$i_{a(0)} = 0{\cdot}207I_a$ at 220V h.t.	9·6mA	14·3mA
$i_{a(pk)} = 3I_a-2i_{a(0)}$	119·4mA	124·1mA
$i_{a(pp)} = i_{a(pk)}-i_{a(0)}$	109·8mA	109·8mA

Transformer Requirements

The value of the transformer secondary inductance for zero initial slope operation is

$$L_s = \frac{R_T\tau}{2} - L_c \text{ (Eq.(3), Appendix 1)}$$

$$= \left(\frac{57{\cdot}5}{2}\times 19-89\right)\text{mH}$$

$$= 546-89 = 457\text{mH}.$$

The transformer turns ratio is given by:

$$n = \frac{i_{s(pp)}}{i_{a(pp)}}\left[1+\frac{L_c}{L_s}\right] \text{ (Eq.(4), Appendix 1)}$$

$$= \frac{0{\cdot}46}{0{\cdot}1098}\left[1+\frac{89}{457}\right] = 5{\cdot}0.$$

This equation does not take into account the transformer iron loss. This was assumed to be 0·5W, which is equivalent to a mean anode current of approximately $0{\cdot}5/200 = 2{\cdot}5mA$ drawn from the valve. Because of the parabolic shape of the anode current waveform this value represents 7·5mA peak-to-peak anode current. Therefore there is only $109{\cdot}8-7{\cdot}5 = 102{\cdot}3mA$ available for scanning, so the transformer turns ratio should be increased by $109{\cdot}8/102{\cdot}3 = 7\%$. This gives n equal to 5·37.

The transformer primary inductance is:

$$L_p = n^2L_s = (5{\cdot}37)^2\times 0{\cdot}457 = 13{\cdot}2H.$$

The transformer primary voltage at the end of scan is:

$$V_p(\tau) = ni_{s(pp)}\left(R_T-\frac{L_s}{\tau}\right) \text{ (Eq.(7), Appendix 1)}$$

$$= 5{\cdot}37\times 0{\cdot}46\times\left(57{\cdot}5-\frac{457}{19}\right) = 82{\cdot}5V.$$

From Fig. 2, the minimum end-of-scan anode voltage necessary to avoid the possibility of bottom cramping at end of life is $59+2 = 61V$. The maximum primary resistance at the lowest h.t. voltage is given by:

$$i_{a(pk)}R_{p(hot)} = h.t._{(min)}-V_k-V_p(\tau)-V_{a(eos)}.$$

Therefore,

$$R_{p(hot)} = \frac{220-18{\cdot}5-82{\cdot}5-61}{0{\cdot}1194} = \frac{58}{0{\cdot}1194} = 485\Omega.$$

If the temperature rise of the transformer above normal ambient is estimated as 50degC, then $1+0{\cdot}00393\Delta T = 1{\cdot}2$. Therefore,

$$R_{p(cold)} = \frac{485}{1{\cdot}2} = 404\Omega.$$

The value of the primary copper loss can now be calculated at 240V h.t.

$$[i_{a(rms)}]^2 = i_{a(pp)}{}^2/5+i_{a(0)}[2\times I_a-i_{a(0)}]$$

$$= \frac{(109{\cdot}8)^2}{5} + 14{\cdot}3[2\times 50{\cdot}9-14{\cdot}3]$$

$$= 0{\cdot}00242+0{\cdot}00125 = 0{\cdot}00367.$$

Therefore,

the primary copper loss $= 0{\cdot}00367\times 404 = 1{\cdot}48W$.

This figure is in agreement with the estimated value of 1·5W. If the estimate was found to be too high, the anode dissipation would be above the maximum value, and the calculations would have to be repeated. If the estimate was low, the anode dissipation would be below its rating and the calculation would be acceptable, although the valve would be under-utilised.

The time at which H_{min} occurs is given by:

$$t_1 = \frac{\tau i_{s(pp)}}{2ni_{a(pp)}} = \frac{19\times 0{\cdot}46}{2\times 5{\cdot}37\times 0{\cdot}1098} = 7{\cdot}4ms.$$

Therefore,

$$i_s(t_1) = i_{s(pp)}\left(\frac{t_1}{\tau}-\frac{1}{2}\right) = 0{\cdot}46\left(\frac{7{\cdot}4}{19}-\frac{1}{2}\right) = -0{\cdot}0506A$$

At max. h.t.,

$$i_a(t_1) = i_a(0)+i_{a(pp)}\left(\frac{t_1}{\tau}\right)^2 = 14{\cdot}2+109{\cdot}8\times 0{\cdot}152$$

$$= 30{\cdot}9mA.$$

The magnetising force is given by

$$H(t) = \frac{0{\cdot}4\pi N_p}{\ell_m}\left[i_a(t)-\frac{i_s(t)}{n}\right].$$

At max. h.t.,

$$H_{(max)} = \frac{0{\cdot}4\pi N_p}{\ell_m}\left[0{\cdot}1241-\frac{0{\cdot}46}{2\times 5{\cdot}37}\right] = 0{\cdot}102\frac{N_p}{\ell_m}\text{ oersted.}$$

$$H_{(min)} = \frac{0{\cdot}4\pi N_p}{\ell_m}\left[0{\cdot}0309+\frac{0{\cdot}0506}{5{\cdot}37}\right] = 0{\cdot}051\frac{N_p}{\ell_m}\text{ oersted.}$$

Transformer Design

The cheapest grade of transformer iron is used with 0·4% silicon content and 0·020 in. laminations. This grade occurs under the trade names Silcor 25, Lamcor 4, or Losil 25. The only advantage of using more expensive silicon iron is to reduce the iron loss in the transformer, which is only a small part of the total losses. There is a considerable advantage in designing the transformer on the smallest possible lamination size because this method reduces the amount of copper required to a minimum.

A common lamination size is the 'waste free' type MEA35 which has a tongue width of 0·75in., a magnetic path length $\ell_m = 4{\cdot}5in.$, and a window area of $1{\cdot}125\times 0{\cdot}375in^2$. (see Fig. 8).

The process of design consists of adjusting the number of turns, wire diameter, number of laminations, and air gap until a primary inductance of 13·2H is obtained; a primary resistance which is equal to, or less than, 404Ω; a secondary resistance of 11·5Ω; and a turns ratio of 5·37.

For $\ell_m = 4{\cdot}5in.$, the values of magnetising force at h.t. max are

$$H_{max} = \frac{0{\cdot}102}{2{\cdot}54\times 4{\cdot}5}N_p = 9{\cdot}0N_p\times 10^{-3}\text{Oe}$$

$$H_{min} = \frac{0{\cdot}051}{2{\cdot}54\times 4{\cdot}5}N_p = 4{\cdot}5N_p\times 10^{-3}\text{Oe}.$$

If a square stack of laminations (3/4in.) is chosen with a stacking factor of 0·96, then 36 laminations are required. By choosing $N_p = 2700$ turns the primary inductance can be calculated with the aid of the sheared B-H curve. The calculations are set out as follows:

2700 turns		
H_{max} =	24·3Oe	
H_{min} =	12·15Oe	
ΔH =	12·15Oe	
ℓ_g =	0·006in.	0·008in.	0·010in.
B_{max} =	13·85kGs	12·06kGs	10·05kGs
B_{min} =	8·00kGs	6·16kGs	5·00kGs
ΔB =	5·85kGs	5·90kGs	5·05kGs

This shows that the value of ℓ_g for maximum permeability is 0·008in., although the increase over 0·006in. is small. However, the iron loss is smaller with the larger gap. The inductance is given by:

$$L_p = \frac{0{\cdot}4\pi N_p{}^2\mu_e\times 10^{-8}\text{H}}{\ell_m}$$

$$= \frac{0{\cdot}4\pi\times(7{\cdot}29\times 10^6)}{(4{\cdot}5\times 2{\cdot}54)}\times\left(\frac{5900}{12{\cdot}15}\right)\times 0{\cdot}75\times 0{\cdot}75\times 0{\cdot}96\times$$

$$\times(2{\cdot}54)^2\times 10^{-8} = 13{\cdot}8H.$$

This figure is sufficiently close to the required value for a first attempt.

The primary resistance and wire gauge must now be calculated.

If a former thickness of $\frac{1}{16}$in. and a clearance of 0·01in. are chosen for the laminations in the former, then the length of the first turn will be:

$$2(\tfrac{3}{4}+0{\cdot}01+\tfrac{1}{16})+2(\tfrac{3}{4}+\tfrac{1}{16}) = 3{\cdot}27in.$$

A good approximation to the length of the mean turn is given by the length of the first turn plus $\pi\times$ the height(h) of the winding. The width of the lamination window is $1\frac{1}{8}$in. The former should have a clearance of $\frac{1}{32}$in., and if $\frac{1}{8}$in. margin is allowed either side of the winding, then the width available for the winding is $(1\frac{1}{8}-\frac{1}{32}-\frac{1}{4}) = 0{\cdot}84in.$

If 40s.w.g. Lewmex F enamelled copper wire is used, then at least 150 turns per layer can be wound in this space. Thus 18 layers for 2700 turns are required, and with 0·002in. paper interleaving, the height of the winding is,

$$h = 0{\cdot}101in.+0{\cdot}036in. = 0{\cdot}137in.$$

The length of the mean turn is

$$3{\cdot}27\text{in.}+\pi\times 0{\cdot}137\text{in.} = 3{\cdot}7\text{in.}$$

The resistance of 40s.w.g. wire is 1·35Ω per yard, so the resistance of the primary winding is,

$$2700\times\frac{3{\cdot}7}{36}\times 1{\cdot}35 = 375\Omega.$$

This resistance is below the required value of 404Ω. If 41s.w.g. wire is used, the resistance is 440Ω, which is too high. Also, there is a disadvantage in using wires finer than 40s.w.g. because of the extra cost of the wire and extra difficulty in winding. Another possibility is to increase the number of turns and decrease the number of laminations. However, the height of the window which is occupied by the primary is

$$(\tfrac{1}{16}+0{\cdot}01+0{\cdot}137) = 0{\cdot}21\text{in.}$$

This value is over half of the available window height (0·375in.) so there would be insufficient room for the secondary winding if the primary winding was increased. A better solution is to wind the secondary winding on first, and the primary afterwards. This winding method increases the primary resistance, so a thicker wire may be necessary. The number of secondary turns required is

$$2700/5{\cdot}37 = 504 \text{ turns.}$$

31s.w.g. is then used.

Secondary

504 turns 31s.w.g.	8 layers at 64 turns/layer	= 0·104in.
Interleaving	8 layers 0·002in. paper	= 0·016in.
	h_s	= 0·120in.

Mean turn = 3·27in.+(π×0·12) = 3·65in.

Resistance $= 504\times\frac{3{\cdot}65}{36}\times 0{\cdot}231 = 11{\cdot}8\Omega$

Primary

2700 turns 39s.w.g.	20 layers at 138 turns/layer	= 0·122in.
Interleaving	20 layers 0·002in. paper	= 0·040in.
Primary-sec. insulation	3 layers 0·002in. paper	= 0·006in.
	h_s	= 0·120in.
	Former	= 0·073in.
	Total build-up	= 0·361in.

Mean turn = 3·65+π(0·361−0·073) = 4·55in.

Resistance of primary $= 2700\times\frac{4{\cdot}55}{36}\times 1{\cdot}151 = 394\Omega.$

This resistance is still slightly low. It might be possible to increase the number of turns slightly and reduce the stack height by one or two laminations, but this would lose the advantage of a square stack of laminations, which is a standard shape for mounting clamps and formers.

The total build-up is 0·361in. which is less than the window height of 0·375in., but only allows a small margin of error for variations in winding methods. It is usual to allow 10% of the window height for this, so the total build-up should not exceed 0·9×0·375in. = 0·338in.

33s.w.g. is then used for the secondary. This leads to a higher value of the resistance R_T, which will lead to a higher L_p. However, L_p is already slightly above the required value of 13·2H.

Secondary

504 turns 33s.w.g.	7 layers at 74 turns/layer	= 0·079in.
Interleaving	7 layers 0·002in. paper	= 0·014in.
	h_s	= 0·093in.

This is 0·027in. less than before, which gives a total build-up of (0·361−0·027)in. = 0·334in., a space factor of 89%.

Mean turn = 3·27+π×0·093in. = 3·56in.

$$\text{Resistance} = 304\times\frac{3{\cdot}56}{36}\times 0{\cdot}311 = 15{\cdot}4\Omega.$$

This means that R_T is increased from 57·5Ω to 61·4Ω. Therefore,

$$L_S = \left(\frac{R_T.\tau}{2} - L_c\right)$$

$$= \frac{61{\cdot}4\times 19}{2} - 89 = 493\text{mH}.$$

Before the new value of the turns ratio, n, is calculated it is necessary to check the estimated value of iron loss.

At 12·06kGs iron loss	= 1·88W/lb
6·16kGs iron loss	= 0·58W/lb
Iron loss	= 1·30/2 = 0·65W/lb .

36 laminations weigh 0·685 lb, so the iron loss is 0·45W. This result is sufficiently close to the estimated value.

The corrected turns ratio is given by:

$$n = \frac{0{\cdot}46}{0{\cdot}1023}\left(1+\frac{89}{493}\right) = 5{\cdot}3.$$

The required transformer primary inductance is now

$$Lp = n^2L_s = (5{\cdot}3)^2\times 0{\cdot}493 = 13{\cdot}8\text{H}.$$

Therefore, 2700 turns give the required inductance. The number of secondary turns has to be increased to

$$\frac{2700}{5{\cdot}3} = 510 \text{ turns.}$$

which can still be accommodated in 7 layers. The value of R_s is now 15·6Ω. The complete transformer specification is given below.

Transformer Specification

Laminations	E and I waste-free pattern with the following manufacturers' numbers; MEA 35, Sankey 70, Baldwin 17, or Scott 120.
Grade	Silcor 25, Lamcor 4, Losil 25, etc., re-annealed.
Thickness	0·020in.
Stack height	0·75in. (36 laminations)
Former	synthetic resin bonded paper tube – wall thickness not to exceed $\frac{1}{16}$in. – length $1\frac{3}{32}$in. – internal dimensions – toleranced to contain 36 laminations $\frac{3}{4}$in. wide. Therefore, the minimum internal dimensions are 0·75in.×0·76in.
Air gap	0·004in. paper spacer; that is, 0·008in. total gap in magnetic path.
Secondary	Wound first. 510 turns 33s.w.g. Lewmex F enamelled copper wire, wound as 6 layers at 74 turns/layer and one layer of 66 turns.
Interleaving	1 turn 0·002in. paper per layer.
Primary-sec.	
Insulation	3 turns 0·002in. paper.
Primary	2700 turns 39s.w.g. Lewmex F enamelled copper wire, wound as 19 layers at 138 turns/layer, and one layer of 78 turns.
Interleaving	1 turn 0·002in. paper per layer.
Impregnation	Okerin 3700 wax.
Build	89% with $\frac{1}{16}$in. former.
Cold resistances	Primary = 397Ω. Secondary = 15·9Ω.

Measurements

The following measurements were carried out using an approximately nominal PCL85 in the timebase circuit shown in Fig. 13. The linearity controls were adjusted for 'zero initial slope' of the anode current waveform, and best linearity on the cathode ray tube. The height control was set for 3% overscan. The cathode resistor required to give the correct anode current was 340Ω.

	Measurements	*Published Data Limits*		
E.H.T.	18	18	18max	kV
H.T.	220	240	—	V
V_{g2}	203·5	220·8	250max	V
V_k	17·5	19·2	—	V
I_k	51·4	56·5	—	mA
I_a	45·9	50·4	—	mA
$i_{a(pk)}$	119	125	—	mA
$i_a(0)$	9	13	*	mA
$i_{a(pp)}$	110	112	—	mA
$i_{a(rms)}$	58	62	—	mA
$V_{a(pk)}$	620	630	2000max	V
$V_{a(eos)}$	62	81	61min	V
p_a	6·3	7·9	8·0max	W
p_{g2}	1·1	1·4	2·0max	W

*Recommended minimum standing anode current = 9mA.

Measurements were also made on a selected 'end-of-life' valve at −10% h.t. (198V). This valve had an emission of 58% of a nominal PCL85, which is less than the defined 'end-of-life' value of 65%. The standing anode current was found to be 1mA. The linearity controls required readjustment, but the non-linearity was better than 5%.

PRACTICAL CIRCUIT DESIGN

The main problem of practical circuit design is to produce a waveform at the grid of the output valve, which is shaped in such a way that the anode current waveform is parabolic, and the scanning current waveform is linear, with a slight s-shaped curvature for wide-angle cathode ray tubes. An increasing positive sawtooth waveform is applied to the grid of the output valve. This sawtooth waveform is usually obtained from the charge and discharge of a capacitor through a high resistance, and the drive circuit may consist of a multivibrator or blocking oscillator. The waveform will be of exponential form, and the curvature is opposite to that required. The shaping of this waveform is the function of the linearity circuits preceding the grid of the output valve. Shaping may be carried out by means of shaping networks or by negative feedback from the deflection coils. The two methods are described in detail in Ref. 9. The feedback method appears to be slightly superior, and it also has the advantage common to feedback amplifiers of reducing variations in performance due to valve and component tolerances.

Negative Feedback

The principle of negative feedback is to apply to the input an opposing voltage proportional to the deflection current. If the amplifier gain is sufficiently high, the deflection current is proportional to the input voltage, so that the linear sawtooth input is required to produce a linear deflection current. The gain which may be obtained from a single output pentode is not sufficient for these theoretical conditions to apply, so some shaping of the input sawtooth or the feedback waveform is necessary.

A feedback voltage proportional to the deflection current can be obtained from a resistor in series with the coils. This method leads to an increase in the transformer size, and an additional stage of amplification is usually required, which tends to make the method uneconomic.

An alternative method is to take the feedback from the anode circuit where an a.c. voltage of large amplitude is present. If a feedback network is used which is the R-C equivalent of the L-R circuit formed by the transformer and coils, then the feedback voltage will be proportional to the deflection current. This method is attributed to Blumlein (Ref. 8) and is very widely used, with numerous variations in the arrangement of the feedback and shaping networks. One method is to use a C-R differentiating circuit followed by an R-C integrating circuit. The differentiating circuit introduces a low frequency attenuation of the feedback voltage, which compensates for the low frequency loss due to the finite transformer inductance. The integrating circuit smooths off and alters the feedback waveform to its required shape, as well as attenuating the high peak anode voltage. The method of calculation of the R-C values is straightforward, but the values obtained are found to require considerable alteration in a practical circuit. Possible reasons for the discrepancy are as follows:

(i) Exponential distortion of the input sawtooth waveform.

(ii) Distortion of the parabolic magnetisation current by variation of the permeability of the core material during scan, and also the non-linear hysteresis loss.

(iii) Curvature of the transfer characteristic of the output valve, which is subject to variation from valve to valve.

(iv) Effect of the cathode decoupling capacitor, which is rarely made large enough to give full decoupling of the cathode resistance.

(v) Possible asymmetry of the deflection coils and the picture tube, and also the s-correction required for wide-angle tubes.

For these reasons, and also to compensate for component tolerances, the resistors in the feedback network are usually made variable, so that the linearity of the raster can be adjusted to its best value.

Flyback Time

The flyback period should be completed between the beginning of the field synchronising pulse sequence and the end of the field blanking period; that is, 1302μs on the 405-line system and 1004μs on the 625-line system. If the flyback period is longer than this, picture information will be received before the flyback is completed, and 'foldover' will occur at the top of the picture. If the flyback period is short, the peak voltages on the valve and transfomer will be high, thus increasing the risk of possible breakdown and failure. Consequently a flyback time of about 600 to 1000μs is commonly used.

An estimate of the flyback time can be made by calculating the effective inductance and resistance on the primary side of the transformer. From Fig. 11 the inductance is L_p in parallel with n^2L_c ; that is,

$$L_{eff} = \frac{L_p n^2 L_c}{L_p + n^2 L_c}.$$

The effective resistance is

$$R_{eff} = r_a R_o / r_a + R_o + R_p + n^2 R_T$$

where R_o is the shunt iron loss and r_a is the a.c. resistance of the valve during flyback. During the flyback period, the current decays exponentially, and the change of current is 95% complete when the exponential is 4·5; that is,

$$\frac{R_{eff}}{L_{eff}} t_o = 4{\cdot}5 \text{ or } t_o = 4{\cdot}5 \frac{L_{eff}}{R_{eff}}.$$

In the transformer design given, $L_p = 13{\cdot}8$H, $L_c = 89$mH, $n = 5{\cdot}3$. Therefore, $L_{eff} = 2{\cdot}1$H, $R_p = 397\Omega$, $R_T = 57{\cdot}5\Omega$, R_o is 40kΩ approx., and r_a is estimated as 15kΩ. This gives $R_{eff} = 12{\cdot}5$kΩ and $t_o = 760\mu$s. These values are of the correct order, but the calculation is only approximate, since the feedback network from the anode to the grid of the output valve is also part of the primary load, and has an effect on the flyback time. However, the influence of the transformer on the flyback time is shown in a qualitative manner.

It should be noted that R_{eff} is mainly determined by r_a , which helps to confirm the assumption made earlier in this article that all the stored energy is dissipated in the valve during flyback. The flyback time of the drive waveform is assumed to be considerably smaller than the flyback time of the output stage. Its maximum value is determined by the duration of the field synchronisation pulse sequence, and is 320μs for either 405- or 625-line systems.

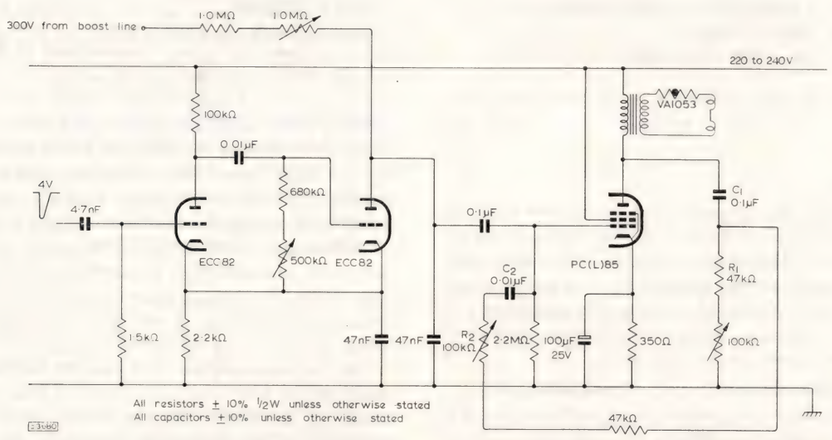


Fig. 13—Practical field timebase

Synchronisation and Interlace

To ensure satisfactory synchronisation and interlace, the trigger pulses applied to the field timebase should have a sharp leading edge with a constant delay relative to the start of the field synchronisation pulse sequence. The delay is necessary since it is not possible to distinguish between the line and field sync pulses until after a period greater than the duration of a line pulse. The delay should be the same on both odd and even frames.

These requirements have to be met in the design of the sync separator stage. However, the correct design of the sync separator does not by itself ensure good interlace. Interlace may be poor or non-existent, if the oscillator flyback time is slightly different on odd or even frames. This difference in flyback time may be caused by line pulses being injected into the field oscillator circuit. The line pulses may be picked up by mutual coupling between the line and field deflection coils, and fed back to the field oscillator via the output transformer and linearity networks. Normally the integrating circuit in the feedback network will suppress these line pulses. However, where this is not effective, any trouble with interlace may be remedied by centre-tapping the secondary of the output transformer and earthing it. Alternatively, two resistors or capacitors may be used across the secondary winding with their centre tap earthed. The use of an earthed screen between the primary and secondary windings may also lead to an improvement.

The layout of the field timebase circuit is also important, and its proximity to the line timebase in the receiver may cause trouble. Cross coupling may also occur in the wiring of double valves common to both line and field timebases.

Practical Circuit

A practical circuit design is shown in Fig. 13, suitable for use with the transformer design given earlier in this article. A double triode multivibrator circuit is used to generate the sawtooth waveform, which is shaped by the feedback network from the anode to grid of the output valve.

ACKNOWLEDGEMENT

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APPENDIX 1

Zero Initial Slope Mode of Operation

The development of the equivalent circuit of the output transformer and deflection coils is shown in Figs. 14 and 11. The real transformer is replaced by an ideal transformer

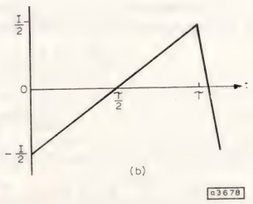

Fig. 14—Deflection coil current

together with R_p , R_s , L_p , $L\ell$ and R_o which represent the transformer resistances, inductances and iron loss respectively. At the comparatively low operating frequency of 50c/s it is a valid approximation to neglect the transformer leakage inductance ($L\ell$) for the small transformers commonly used. The accuracy of this approximation may be checked from the formula given in Fig. 8.

For the purpose of deriving the required design equations, the transformer iron loss R_o is neglected. This is re-introduced as a correction term as described on page 182.

Magnetising Current

From Fig. 11(c)

$$V_p(t) = L_p \frac{di_o(t)}{dt} = n^2 R_T \frac{i_s(t)}{n} + n^2 L_c \frac{d}{dt}\left(\frac{i_s(t)}{n}\right).$$

But,

$$i_s(t) = i_{s(pp)}\left(\frac{t}{\tau} - \frac{1}{2}\right),$$

therefore

$$\frac{d}{dt}\left(\frac{i_s(t)}{n}\right) = \frac{i_{s(pp)}}{\tau}.$$

Therefore,

$$V_p(t) = L_p \frac{di_o(t)}{dt} = nR_T i_{s(pp)}\left(\frac{t}{\tau} - \frac{1}{2}\right) + \frac{nL_c}{\tau} i_{s(pp)} \quad \ldots(1)$$

$$i_o(t) = \frac{1}{L_p}\int_0^t [V_p(t)]dt$$

$$= \frac{1}{L_p}\int_0^t \left[nR_T i_{s(pp)}\left(\frac{t}{\tau} - \frac{1}{2}\right) + nL_c \frac{i_{s(pp)}}{\tau}\right]dt$$

$$= \frac{ni_{s(pp)}}{L_p}\left[R_T\left(\frac{t^2}{2\tau} - \frac{t}{2}\right) + \frac{L_c t}{\tau}\right] + A$$

where A is a constant.

Anode Current

$$i_a(t) = i_o(t) + \frac{i_s(t)}{n}$$

$$= \frac{ni_{s(pp)}}{L_p}\left[R_T\left(\frac{t^2}{2\tau} - \frac{t}{2}\right) + \frac{L_c t}{\tau}\right] + A + \frac{i_{s(pp)}}{n}\left[\frac{t}{\tau} - \frac{1}{2}\right]$$

At t = 0,

$$i_a(t) = i_a(0)$$

therefore,

$$A = i_a(0) + \frac{i_{s(pp)}}{2n}.$$

Therefore,

$$i_a(t) = i_a(0) + \frac{i_{s(pp)}}{n}\frac{t}{\tau} + \frac{ni_{s(pp)}}{L_p}\left[R_T\left(\frac{t^2}{2\tau} - \frac{t}{2}\right) + \frac{L_c t}{\tau}\right]. \quad \ldots(2)$$

It may be seen that in general the anode current waveform is parabolic. For an ideal transformer, L_p is infinite, and the second order terms vanish: $i_a(t)$ is thus a linear sawtooth.

Zero Initial Slope Conditions

$$\frac{di_a(t)}{dt} = \frac{i_{s(pp)}}{n\tau} + \frac{ni_{s(pp)}}{L_p}\left[R_T\left(\frac{t}{\tau} - \frac{1}{2}\right) + \frac{L_c}{\tau}\right]$$

$$= \frac{ni_{s(pp)}}{L_p}\left[R_T\left(\frac{t}{\tau} - \frac{1}{2}\right) + \frac{L_c}{\tau} + \frac{L_p}{n^2\tau}\right].$$

Substituting $L_p = n^2 L_s$

$$\frac{di_a(t)}{dt} = \frac{ni_{s(pp)}}{L_p}\left[R_T\left(\frac{t}{\tau} - \frac{1}{2}\right) + \frac{L_c + L_s}{\tau}\right]$$

$$= 0 \text{ when } t = \frac{\tau}{2} - \frac{L_c + L_s}{R_T}.$$

The second derivative $\frac{d^2 i_a(t)}{dt^2}$ is positive, hence this indicates

a minimum value at t = 0; that is, at the start of scan

$$L_c+L_s = \frac{R_T\tau}{2}. \qquad \ldots(3)$$

Turns Ratio

Substitute for $R_T = \frac{2(L_c+L_s)}{\tau}$ in the equation for $i_a(t)$. from Eq.(2).

$$i_a(t) = i_a(0) + \frac{i_{s(pp)}}{n}\frac{t}{\tau} + \frac{ni_{s(pp)}}{n^2L_s}\left[\frac{2(L_c+L_s)}{\tau}\left(\frac{t^2}{2\tau}-\frac{t}{2}\right)+\frac{L_ct}{\tau}\right]$$

$$= i_a(0) + \frac{i_{s(pp)}}{n}\left[\frac{2}{\tau}\left(1+\frac{L_c}{L_s}\right)\left(\frac{t^2}{2\tau}-\frac{t}{2}\right)+\frac{t}{\tau}\left(1+\frac{L_c}{L_s}\right)\right].$$

At the end of scan $t = \tau$ and therefore:

$$i_{a(pp)} = i_a(\tau)-i_a(0) = \frac{i_{s(pp)}}{n}\left(1+\frac{L_c}{L_s}\right).$$

Hence the transformer turns ratio n is given by:

$$n = \frac{i_{s(pp)}}{i_{a(pp)}}\left[1+\frac{L_c}{L_s}\right]. \qquad \ldots(4)$$

Substitute for n in the equation for $i_a(t)$

$$i_s(t) =$$

$$i_a(0) + \frac{i_{s(pp)}}{\frac{i_{s(pp)}}{i_{a(pp)}}\left(1+\frac{L_c}{L_s}\right)}\left[\frac{2}{\tau}\left(1+\frac{L_c}{L_s}\right)\left(\frac{t^2}{2\tau}-\frac{t}{2}\right)+\frac{t}{\tau}\left(1+\frac{L_c}{L_s}\right)\right]$$

or

$$i_a(t) = i_a(0)+i_{a(pp)}\left(\frac{t}{\tau}\right)^2. \qquad \ldots(5)$$

The average anode current

$$I_a = \frac{1}{\tau}\int_0^\tau (i_a(t))dt \text{ during scan}$$

$$= \frac{1}{\tau}\int_0^\tau \left[i_a(0)+i_{a(pp)}\left(\frac{t}{\tau}\right)^2\right]dt$$

$$= i_a(0) + \frac{1}{\tau}i_{a(pp)}\left[\frac{t^3}{3\tau^2}\right]_0^\tau.$$

Therefore,

$$I_a = i_a(0) + \frac{1}{3}i_{a(pp)}.$$

If the anode current during flyback can be assumed to be parabolic, then the average current for the whole scanning period is:

$$I_a = i_a(0) + \frac{1}{3}i_{a(pp)}. \qquad \ldots(6)$$

Transformer Voltage

$$V_p(t) = nR_Ti_{s(pp)}\left(\frac{t}{\tau}-\frac{1}{2}\right)+\frac{nL_c}{\tau}i_{s(pp)} \text{ from Eq.(1),}$$

$$= \frac{ni_{s(pp)}}{\tau}\left[R_T\left(t-\frac{\tau}{2}\right)+L_c\right]$$

$$= \frac{ni_{s(pp)}}{\tau}(R_T\tau-L_s)$$

since

$$\frac{R_T\tau}{2} = L_c+L_s.$$

At the end of scan $t = \tau$. Therefore,

$$V_p(\tau) = ni_{s(pp)}\left(R_T-\frac{L_s}{\tau}\right). \qquad \ldots(7)$$

R.M.S. Secondary Current

$i_s(t) = i_{s(pp)}\left[\frac{t}{\tau}-\frac{1}{2}\right]$ during scan. Therefore,

$$[i_{s(rms)}]^2 = \frac{1}{\tau}\int_0^\tau [i_s(t)]^2dt$$

$$= \frac{1}{\tau}\int_0^\tau [i_{s(pp)}]^2\left[\frac{t}{\tau}-\frac{1}{2}\right]^2dt$$

$$= \left[i_{s(pp)}\right]^2\frac{\tau}{3}\left[\left(\frac{t}{\tau}-\frac{1}{2}\right)^3\right]_0^\tau$$

$$= \left[\frac{i_{s(pp)}}{12}\right]^2.$$

If the flyback current can be considered linear, it has a similar formula. Therefore,

$$i_{s(rms)} = \frac{i_{s(pp)}}{\sqrt{12}} \qquad \ldots(8)$$

This equation applies to an ideal sawtooth waveform. For modern wide-angle cathode ray tubes, a certain amount of rounding-off of the waveform (s-correction) is required to compensate for tube curvature. A better estimate of $i_{s(rms)}$ is given by:

$$i_{s(rms)} = \frac{i_{s(pp)}}{\sqrt{10}} \qquad \ldots(9)$$

for 110° cathode ray tubes.

R.M.S. Anode Current

$$i_a(t) = i_a(0)+i_{a(pp)}\left(\frac{t}{\tau}\right)^2$$

therefore,

$$[i_{a(rms)}]^2 = \frac{1}{\tau}\int_0^\tau [i_a(t)]^2dt$$

$$= \frac{1}{\tau}\int_0^\tau \left[[i_a(0)]^2+2i_a(0)i_{a(pp)}\left(\frac{t}{\tau}\right)^2+[i_{a(pp)}]^2\left(\frac{t}{\tau}\right)^4\right]dt$$

$$= i_a(0)^2+\frac{1}{5}[i_{a(pp)}]^2+\frac{2}{3}i_a(0)i_{a(pp)}.$$

Substituting for $i_{a(pp)}$ in terms of I_a,

$$i_{a(pp)} = 3[I_a-i_a(0)].$$

Therefore,

$$[i_{a(rms)}]^2 = \frac{1}{5}[i_{a(pp)}]^2+i_a(0)[2I_a-i_a(0)]. \qquad \ldots(10)$$

Magnetising Force

The instantaneous core magnetisation is the algebraic sum of the primary and secondary ampere-turns: that is,

$$H(t) = \frac{0{\cdot}4\pi}{\ell_m}[N_pi_a(t)-N_si_s(t)]$$

$$= \frac{0{\cdot}4\pi}{\ell_m}N_p\left[i_a(t)-\frac{1}{n}i_s(t)\right].$$

Substituting the expressions for $i_a(t)$ and $i_s(t)$

$$H(t) = \frac{0{\cdot}4\pi}{\ell_m}N_p\left[i_a(0)+i_{a(pp)}\left(\frac{t}{\tau}\right)^2-\frac{i_{s(pp)}}{n}\left(\frac{t}{\tau}-\frac{1}{2}\right)\right]$$

$$\frac{dH(t)}{dt} = \frac{0{\cdot}4\pi N_p}{\ell_m}\left[2i_{a(pp)}\frac{t}{\tau^2}-\frac{i_{s(pp)}}{n\tau}\right]$$

$\frac{d^2H(t)}{dt^2}$ is positive, therefore the minimum value of H(t) occurs at a time t_1 such that:

$$2i_{a(pp)}\frac{t_1}{\tau^2} = \frac{i_{s(pp)}}{n\tau}$$

or

$$t_1 = \frac{i_{s(pp)}}{2ni_{a(pp)}}\tau. \qquad \ldots(11)$$

The maximum value of H(t) occurs at the end of scan when $t = \tau$, that is,

$$H_{(max)} = \frac{0{\cdot}4\pi N_p}{\ell_m}\left[i_{a(pk)}-\frac{i_{s(pp)}}{2n}\right] \qquad \ldots(12)$$

$$H_{(min)} = \frac{0{\cdot}4\pi N_p}{\ell_m}\left[i_a(t_1)-\frac{i_s(t_1)}{n}\right] \qquad \ldots(13)$$

where,

$$i_a(t_1) = i_{a(pp)}\left(\frac{t_1}{\tau}\right)^2$$

and

$$i_s(t_1) = i_{s(pp)}\left(\frac{t_1}{\tau}-\frac{1}{2}\right).$$

APPENDIX 2
Temperature Rise of the Output Transformer

During operation, the transformer must dissipate all the power due to the anode current that is not dissipated in the output valve, the cathode resistor, and the deflection coils. The transformer will warm up until the internally generated heat is equal to the sum of the amounts of heat which can be dissipated by radiation and convection. A steady operating temperature will be reached when the heat loss is equal to the heat gained.

Losses by conduction to any metal object that the transformer may be mounted on will not be considered. Any metal surface immediately under the transformer will be considered as a continuation of the transformer surface for calculation of radiation and convection losses.

The amount of heat radiated by a hot body is dependent upon the ambient temperature and the emissivity of the outer surface. An emissivity value of 0·95 may be taken as an average value for the complete transformer.

The heat distribution in the transformer will depend upon the density and thermal conductivity of the various materials used in its construction. Copper has a better conductivity than that of iron, and also a higher density. The interleaving paper, enamel, former material, and impregnating compound, will have a relatively low density, and the overall effect is to give the finished transformer an average density almost equal to that of the iron. The transformer will therefore be treated as a homogeneous body, and the internal temperature gradient neglected.

Convection Loss

If a body is cooled by natural convection, the rate of loss of heat from its surface is stated by Blume (Ref. 7) to be:

$$W_c = 1{\cdot}4\times10^{-3}(T_2-T_1)W/in^2$$

where (T_2-T_1) is the excess temperature of the surface, in degrees C, over its surroundings. The formula was derived from consideration of the convection loss of a plane vertical surface.

In practice, if a transformer is mounted with the laminations in a vertical plane, the top horizontal surface will lose heat at a rate 15 to 20% faster than the vertical sides. This heat loss is offset by the fact that the convection loss of horizontal surfaces on the underside of the transformer will be less than that of the vertical sides, because the hot air will have to flow across the lower surfaces to escape.

The effective cooling area for convection is the actual surface of the body – to a close approximation – provided that the surface is not too irregular. A transformer will normally comply with this requirement.

For a wasteless E-I lamination, fully wound, as shown in Fig. 15, the surface area is:

$$A_c = 22aS+81a^2$$

where a is the E-I variable (tongue width), and S the stack height.

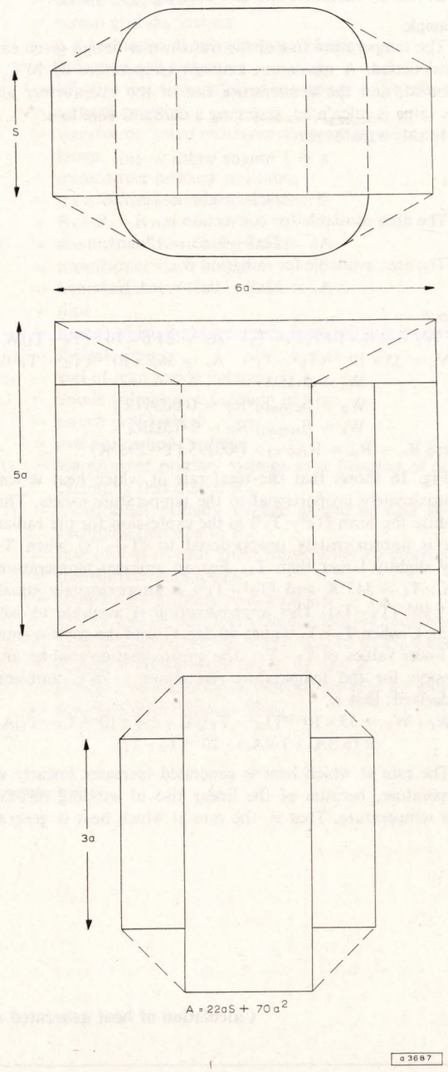

Fig. 15—Effective cooling area for radiation

Radiation Loss

The effective radiating surface of a body is the outside surface of its envelope, regardless of shape. This envelope is that which would be produced by covering the body with thin cords, stretched tightly around it.

For a better visual explanation, consider the radiating surface formed by the three surfaces of a cube at a corner, when viewed from inside the cube. Each surface will radiate into the same solid angle, but the amount of radiation received by the observer will be that due to an area formed by a perspective view of the corner drawn on a plane surface.

The value of effective radiating area may be derived from Fig. 15 for a fully wound E-I wasteless lamination without end sheets, as shown in Fig. 15.

$$A_r = 22aS+70a^2.$$

The radiation from a black body (E = 1) is given by the Stefan-Boltzmann fourth power law of radiation,

$$W_r = KE(T_2^4-T_1^4)W/\text{unit area},$$

where (T_2-T_1) is the excess temperature of the body over its surrounds, measured in °K.

The constant, K, is $5{\cdot}709\times10^{-5}$ergcm^{-2}.deg^{-4}K.sec.$^{-1}$

$$1W = 10^7\text{ergsec}^{-1}$$

$$K = 5{\cdot}709\times10^{-12}\text{Wcm}^{-2}\text{deg}^{-4}\text{K}$$

$$= 36{\cdot}82\times10^{-12}\text{Win}^{-2}\text{deg}^{-4}\text{K}.$$

If the emissivity of a typical transformer may be taken as 0·95, then:

$$W_r = 35\times10^{-12}(T_2^4-T_1^4)Win^{-2}.$$

Total loss by radiation and convection $= W_r+W_c$.

Example

The temperature rise of the transformer design given earlier is calculated. A maximum ambient temperature of 70°C was assumed, and the temperature rise of the transformer above this value is calculated, assuming a constant core loss.

In this transformer:

$$a = \tfrac{1}{2} \text{ tongue width} = \tfrac{3}{8}in;$$

and

$$S = \text{stack height} = \tfrac{3}{4}in.$$

The area available for convection is

$$A_c = 22aS+81a^2 = 17{\cdot}6in^2.$$

The area available for radiation is

$$A_r = 22aS+70a^2 = 161{\cdot}1in^2$$

Hence

$$W_c = 1{\cdot}4\times10^{-3}(T_2-T_1) \quad A_c = 24{\cdot}6\times10^{-3}(T_2-T_1)W$$
$$W_r = 35\times10^{-12}(T_2^4-T_1^4) \quad A_r = 565\times10^{-12}(T_2^4-T_1^4)W$$
$$W_i = 0{\cdot}45W$$
$$W_p = [i_{a(rms)}]^2R_p = 0{\cdot}00367R_p$$
$$W_s = [i_{s(rms)}]^2R_s = 0{\cdot}0202R_s$$

where $R_s = R_p = R_{(20°C)}\times1{\cdot}00393\ (T-293°K)$

Fig. 16 shows that the total rate at which heat is lost is approximately proportional to the temperature excess. This is because the term $(T_2^4-T_1^4)$ in the expression for the radiation loss is approximately proportional to (T_2-T_1) when T_2 is only slightly larger than T_1. For an ambient temperature of 70°C, $T_1 = 343°K$ and $(T_2^4-T_1^4)$ is approximately equal to $1{\cdot}8\times10^8\ (T_2-T_1)$. This approximation is accurate to within 4 deg. C when T_2-T_1 equals 40 deg. C; and the error is smaller for lower values of T_2-T_1. The approximation enables an expression for the temperature rise above a 70°C ambient to be derived: that is,

$$W_r+W_c = 35\times10^{-12}[T_2^4-T_1^4]A_r+1{\cdot}4\times10^{-3}(T_2-T_1)A_c$$
$$\simeq (6{\cdot}3A_r+1{\cdot}4A_c)\times10^{-3}(T_2-T_1).$$

The rate at which heat is generated increases linearly with temperature, because of the linear rise of winding resistance with temperature. That is, the rate at which heat is generated is:

$$W_i+1{\cdot}2[W_{p(20°C)}+W_{s(20°C)}][1+0{\cdot}00393(T_2-T_1)].$$

By equating these two expressions and solving for T_2-T_1

$$T_2-T_1 = \frac{W_i+1{\cdot}2[W_{p(20°C)}+W_{s(20°C)}]}{(6{\cdot}3A_r+1{\cdot}4A_c)\times10^{-3}-0{\cdot}00472[W_{p(20°C)}+W_{s(20°C)}]}$$

The approximation gives a conservative estimate of the temperature rise, because the curvature of the true radiation law $(T_2^4-T_1^4)$ would make the true W_r+W_c curve cut the $(W_i+W_p+W_s)$ curve at a lower value of T_2-T_1 (Fig. 16). For the example

$$T_2-T_1 = \frac{0{\cdot}45+1{\cdot}2(1{\cdot}44+0{\cdot}32)}{(101+24{\cdot}6)\times10^{-3}-8{\cdot}3\times10^{-3}} = \frac{2{\cdot}55}{0{\cdot}117} = 21{\cdot}8°C.$$

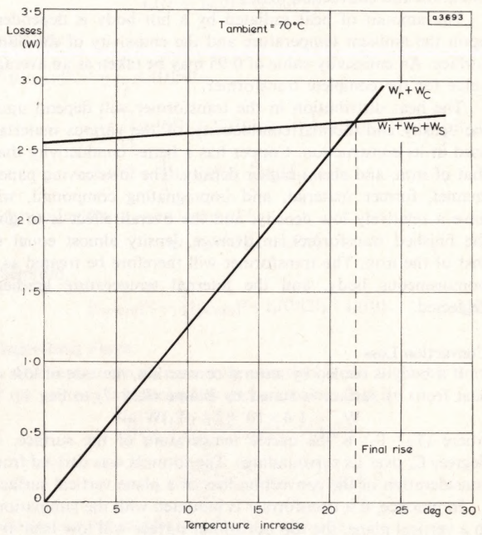

Fig. 16—Transformer temperature rise

TABLE 1

Calculation of heat generated and heat lost by radiation and convection

T	T − 343°K	T − 293°K	1+0·00393 (T − 293°K)	R_p (Ω)	W_p (W)	R_s (Ω)	W_s (W)	$W_i+W_p+W_s$ (W)	$T_2^4-T_1^4$ 10^{10}	W_r (W)	W_c (W)	W_r+W_c (W)
343	0	50	1·197	472	1·731	18·7	0·378	2·559	0	0	0	0
348	5	55	1·216	480	1·760	19·0	0·384	2·594	0·0831	0·469	0·123	0·592
353	10	60	1·236	486	1·782	19·3	0·390	2·622	0·1693	0·956	0·246	1·202
358	15	65	1·256	495	1·818	19·6	0·396	2·664	0·2591	1·465	0·369	1·834
363	20	70	1·275	503	1·848	19·9	0·402	2·700	0·3529	1·992	0·492	2·484

Curves of $(W_i+W_p+W_s)$ and (W_r+W_c) as a function of temperature rise cross each other at the final rise in temperature, that is, 21·8degC from Fig. 16.

LIST OF SYMBOLS USED IN THE ARTICLE

A_r = effective radiation area
a = half the tongue width of transformer laminations (see Fig. 8)
A_c = effective cooling area for convection
B = peak transformer flux density (gauss)
h = transformer winding height
H = transformer magnetising force (oersted)
$i_a(0)$ = standing anode current for a Z.I.S. design
$i_{a(pk)}$ = peak anode current
$i_{a(pp)}$ = peak-to-peak anode current
$i_{a(pp)}'$ = peak-to-peak anode current corrected for iron loss
$i_{a(rms)}$ = r.m.s. anode current
$i_a(t)$ = anode current as a function of time
I_a = average anode current
I_k = average cathode current
I_L = transformer iron loss current (average value)
$i_o(t)$ = transformer magnetising current as a function of time
i_s = secondary scanning current
$i_{s(pp)}$ = peak-to-peak secondary scanning current
$i_{s(rms)}$ = r.m.s. secondary scanning current
ℓ_g = total air gap in transformer core
ℓ_m = magnetic path length of transformer
L_c = deflection coil inductance
L_{eff} = effective inductance referred to primary of transformer
L_ℓ = transformer leakage inductance referred to the secondary
L_p = transformer primary inductance
L_s = transformer secondary inductance
n = transformer turns ratio
N_p = number of turns in primary winding of the transformer
N_s = number of turns in secondary winding of the transformer
p_a = anode dissipation
p_{g2} = screen grid dissipation
r_a = a.c. resistance of valve during flyback
R_c = deflection coil resistance
R_{eff} = effective resistance referred to primary of transformer
R_k = cathode resistor
R_o = transformer shunt resistance representing average core losses
R_p = transformer primary resistance
R_s = transformer secondary resistance
R_T = $R_s+R_c+R_{Th}$
R_{Th} = nominal thermistor resistance
S = transformer stack height
T = temperature in °K
t = time
t_1 = time at which the magnetising force H(t) is a minimum
t_o = flyback time
$v_{a(eos)}$ = end of scan anode voltage
$V_a(t)$ = anode voltage as a function of time
V_{g2} = screen grid voltage
V_k = average cathode voltage
$V_p(t)$ = transformer primary voltage as a function of time, excluding that due to R_p
$V_p(\tau)$ = transformer primary voltage at end of scan ($t=\tau$) excluding that due to R_p
W_c = rate of loss of heat from transformer by convection
W_i = transformer core losses
W_p = transformer primary resistance loss
W_r = rate of loss of heat from transformer by radiation
W_s = total dissipation on secondary side of transformer
ΔT = change in temperature deg. C or deg. K
μ_e = effective permeability of transformer plus air gap
τ = scanning time taken as 19ms

Field Timebases for 20kV Deflection

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The design of a field output transformer and three practical field timebase circuits suitable for 20kV scanning requirements are described. A PCL85 field output valve is used at its new anode dissipation of 8W, with the use of 220V to 240V h.t. supplies.

INTRODUCTION

The design of a field output transformer suitable for operation with a stabilised line timebase from 220V to 240V is discussed. A PCL85 field output valve is used at its new anode dissipation rating of 8W, with a standing anode current of 8% of the peak current. The design is based on the 'Zero Initial Slope' mode of operation described in the preceding article.

Three practical timebase circuits are given; multivibrator drive, blocking oscillator drive, and a self-oscillator circuit.

The increase in the anode dissipation rating of the PCL85, together with the reduction in standing anode current, enables 20kV scanning requirements to be met with an output transformer of reasonable size.

PRACTICAL FIELD TIMEBASE CIRCUITS

The circuit diagrams of three practical field timebase circuits are given in Figs. 1, 2, 3. The same output transformer is used in each case.

The multivibrator and blocking oscillator circuits follow conventional practice. In the self-oscillating circuit, the flyback pulse on the anode of the output valve is attenuated and shaped, and applied to the grid of the triode. The whole circuit forms a multivibrator, the frequency of which is determined by the time-constant in the grid circuit of the triode. As usual with this type of circuit, it may be necessary to take precautions to prevent line pulses from reaching the grid of the triode via the back-coupling from the anode, which could lead to poor interlace. The prototype circuit is satisfactory in this respect, but any trouble with interlace may be remedied by centre-tapping the secondary of the output transformer and earthing it. Alternatively, two resistors or capacitors may be used across the secondary winding with their centre-tap earthed. The use of an earthed screen between the primary and secondary windings may also lead to an improvement.

OPERATION OF THE FIELD OUTPUT VALVE PCL85 (pentode section)

The following measurements were carried out with the use of a nominal PCL85 in the timebase circuit (Fig. 1). Similar results apply to the other circuits. The linearity controls were adjusted for 'zero initial slope' of the anode current waveform, and best linearity on the cathode ray tube. The height control was set for 3% overscan. The required cathode resistor is 330Ω±5%.

	Measurements		*Published Data Limits*	
E.H.T.	20	20	20 max	kV
H.T.	220	240	—	V
V_{g2}	202	221	250 max	V
V_k	17·6	19·1	—	V
I_k	53·4	58	—	mA
I_a	47	51·1	—	mA
$i_{a(pk)}$	125	130	—	mA
$i_a(0)$	10	14	*	mA
$i_{a(pp)}$	115	116	—	mA
$i_{a(rms)}$	59	62·5	—	mA
$v_{a(pk)}$	720	740	2000 max	V
$V_{a(eos)}25°C$	62	80	—	V
$V_{a(eos)}75°C$	59	77	58(min)	V
p_a	6·3	7·9	8·0 max	W
p_{g2}	1·3	1·5	2·0 max	W

Measurements were also made on a selected 'end of life' valve at −10% h.t. (198V). This valve had an emission of 58% of a nominal PCL85, which is less than the defined 'end of life' value of 65%. The peak anode current was found to be 110mA, and the standing anode current was 2mA. The linearity controls required re-adjustment, but the non-linearity was better than 5%.

*The recommended minimum standing anode current is 10mA.

DEFLECTION COILS

The deflection coils used are the Plessey type TLA20240, catalogue number 413/1/00011/001. This type number refers to a field coil resistance of 38Ω, and an 8Ω thermistor is used for temperature compensation.

Inductance	L_c	= 89mH
Resistance	R_c	= 38Ω
Thermistor	R_{Th}	= 8Ω at 25°C (Mullard type VA1053)
Scanning current $I_{s(pp)}$		= 0·47A
E.H.T.		= 20kV
Cathode ray tube		= AW47-91
Vertical deflection		= 30·4cm
$I_{s(pp)}$ for 3% overscan		= 0·48A
$I_{s(rms)}$ for 3% overscan		= 0·15A

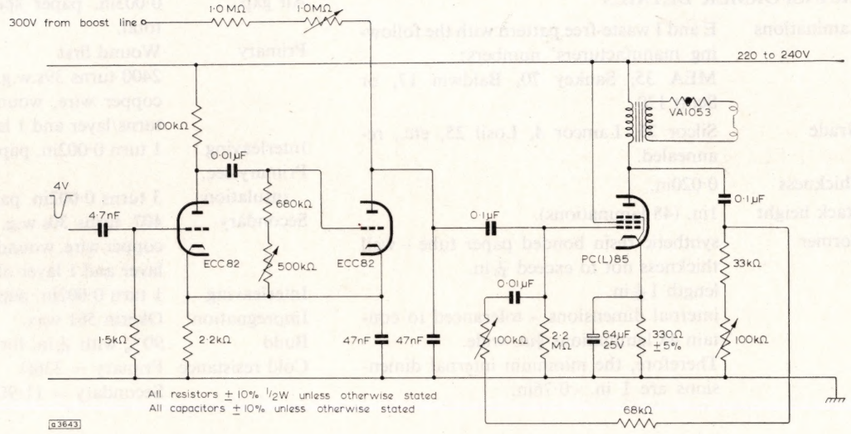

Fig. 1—
Field output stage for 20kV multivibrator drive

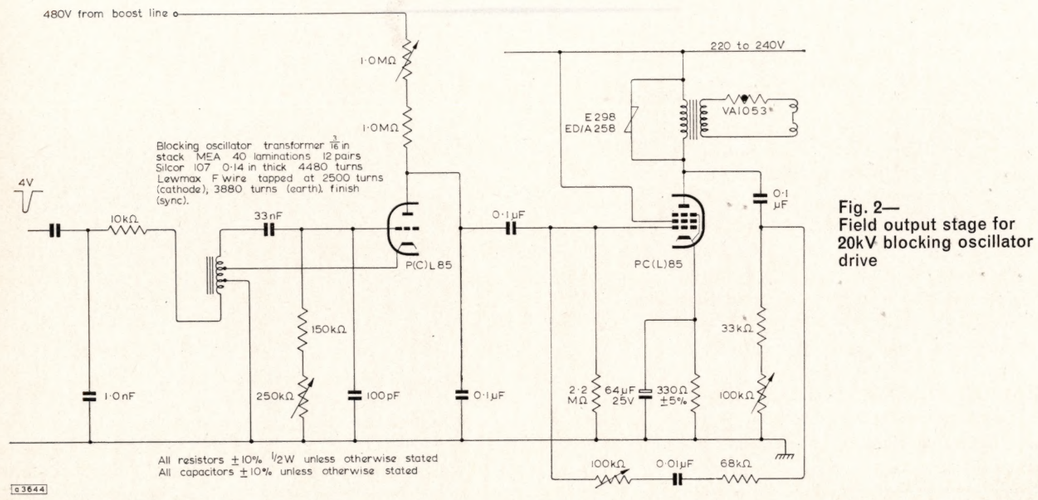

Fig. 2—
Field output stage for 20kV blocking oscillator drive

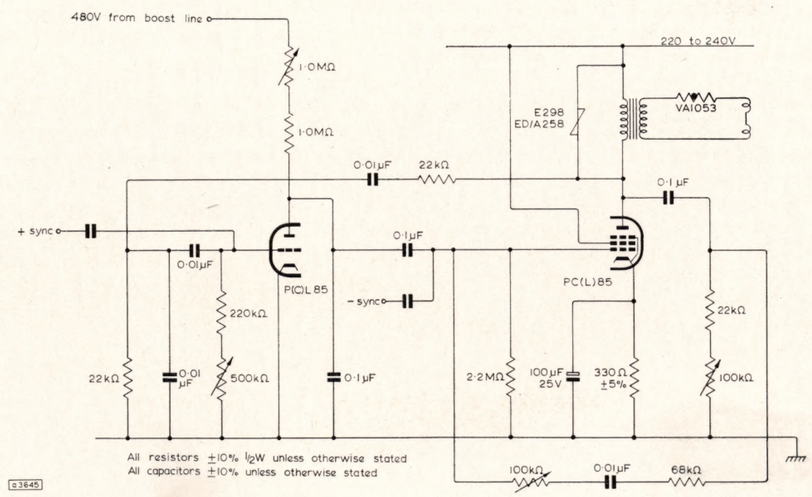

Fig. 3—
Field output stage for 20kV self-oscillating circuit

TRANSFORMER DETAILS

Laminations	E and I waste-free pattern with the following manufacturers' numbers: MEA 35, Sankey 70, Baldwin 17, or Scott 120.
Grade	Silcor 25, Lamcor 4, Losil 25, etc., re-annealed.
Thickness	0·020in.
Stack height	1in. (48 laminations).
Former	synthetic resin bonded paper tube – wall thickness not to exceed $\frac{1}{16}$in. length 1$\frac{3}{32}$in. internal dimensions – toleranced to contain 48 laminations $\frac{3}{4}$in. wide. Therefore, the minimum internal dimensions are 1 in.×0·76in.
Air gap	0·003in. paper spacer; that is, 0·006in. total.
Primary	Wound first 2400 turns 39s.w.g. Lewmex F enamelled copper wire, wound as 17 layers at 138 turns/layer and 1 layer of 54 turns.
Interleaving	1 turn 0·002in. paper per layer.
Primary-sec. insulation	3 turns 0·002in. paper.
Secondary	407 turns 30s.w.g. Lewmex F enamelled copper wire, wound as 6 layers at 60 turns/layer and 1 layer of 47 turns.
Interleaving	1 turn 0·002in. paper per layer.
Impregnation	Okerin 561 wax.
Build	90% with $\frac{1}{16}$in. former.
Cold resistance	Primary = 336Ω Secondary = 11·9Ω.